Shen-Iuan Liu

List of Publications by Year
in descending order

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249 papers	4,586 citations	126708 33 h-index	149479 56 g-index
249 all docs	249 docs citations	249 times ranked	2175 citing authors

#	Article	IF	Citations
1	A Broadband Noise-Canceling CMOS LNA for 3.1â€“10.6-GHz UWB Receivers. IEEE Journal of Solid-State Circuits, 2007, 42, 329-339.	3.5	325
2	CMOS wideband amplifiers using multiple inductive-series peaking technique. IEEE Journal of Solid-State Circuits, 2005, 40, 548-552.	3.5	141
3	An Ultra-Wide-Band 0.4–10-GHz LNA in 0.18-<formula formulatype="inline"><tex>mu</tex></formula>m CMOS. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 217-221.	2.3	140
4	A wide-range delay-locked loop with a fixed latency of one clock cycle. IEEE Journal of Solid-State Circuits, 2002, 37, 1021-1027.	3.5	137
5	A 40â€“550 MHz Harmonic-Free All-Digital Delay-Locked Loop Using a Variable SAR Algorithm. IEEE Journal of Solid-State Circuits, 2007, 42, 361-373.	3.5	132
6	Miniature 3-D inductors in standard CMOS process. IEEE Journal of Solid-State Circuits, 2002, 37, 471-480.	3.5	119
7	Inductorless Wideband CMOS Low-Noise Amplifiers Using Noise-Canceling Technique. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 305-314.	3.5	108
8	40 Gb/s Transimpedance-AGC Amplifier and CDR Circuit for Broadband Data Receivers in 90 nm CMOS. IEEE Journal of Solid-State Circuits, 2008, 43, 642-655.	3.5	98
9	A spread-spectrum clock generator with triangular modulation. IEEE Journal of Solid-State Circuits, 2003, 38, 673-676.	3.5	95
10	Clock-deskew buffer using a SAR-controlled delay-locked loop. IEEE Journal of Solid-State Circuits, 2000, 35, 1128-1136.	3.5	91
11	New dynamic flip-flops for high-speed dual-modulus prescaler. IEEE Journal of Solid-State Circuits, 1998, 33, 1568-1571.	3.5	89
12	A Digital Calibration Technique for Charge Pumps in Phase-Locked Systems. IEEE Journal of Solid-State Circuits, 2008, 43, 390-398.	3.5	87
13	Fast-switching frequency synthesizer with a discriminator-aided phase detector. IEEE Journal of Solid-State Circuits, 2000, 35, 1445-1452.	3.5	82
14	Analysis of on-chip spiral inductors using the distributed capacitance model. IEEE Journal of Solid-State Circuits, 2003, 38, 1040-1044.	3.5	78
15	A wide-range and fast-locking all-digital cycle-controlled delay-locked loop. IEEE Journal of Solid-State Circuits, 2005, 40, 661-670.	3.5	70
16	A broadband noise-canceling CMOS LNA for 3.1-10.6-GHz UWB receiver. , 0, , .		68
17	A 2.5 GHz All-Digital Delay-Locked Loop in 0.13 $mu{hbox {m}}$ CMOS Technology. IEEE Journal of Solid-State Circuits, 2007, 42, 2338-2347.	3.5	67
18	A 2.4-GHz Subharmonically Injection-Locked PLL With Self-Calibrated Injection Timing. IEEE Journal of Solid-State Circuits, 2013, 48, 417-428.	3.5	62

#	Article	IF	Citations
19	A 1.5 GHz All-Digital Spread-Spectrum Clock Generator. IEEE Journal of Solid-State Circuits, 2009, 44, 3111-3119.	3.5	54
20	A 155.52 Mbpsâ€“3.125 Gbps Continuous-Rate Clock and Data Recovery Circuit. IEEE Journal of Solid-State Circuits, 2006, 41, 1380-1390.	3.5	52
21	A Submicrowatt 1.1-MHz CMOS Relaxation Oscillator With Temperature Compensation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 837-841.	2.2	51
22	A 40 Gb/s CMOS Serial-Link Receiver With Adaptive Equalization and Clock/Data Recovery. IEEE Journal of Solid-State Circuits, 2008, 43, 2492-2502.	3.5	47
23	A spur-reduction technique for a 5-GHz frequency synthesizer. IEEE Transactions on Circuits and Systems I: Regular Papers, 2006, 53, 526-533.	3.5	46
24	Sinusoidal oscillators with single element control using a current-feedback amplifier. International Journal of Electronics, 1994, 77, 1007-1013.	0.9	45
25	Pseudo-exponential function for MOSFETs in saturation. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2000, 47, 1318-1321.	2.3	44
26	A 0.7â€“2-GHz Self-Calibrated Multiphase Delay-Locked Loop. IEEE Journal of Solid-State Circuits, 2006, 41, 1051-1061.	3.5	44
27	A Fully Differential Comparator-Based Switched-Capacitor $DeltaSigma$ Modulator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 369-373.	2.2	44
28	A 0.5â€“5-GHz Wide-Range Multiphase DLL With a Calibrated Charge Pump. IEEE Transactions on Circuits and Systems II: Express Briefs, 2007, 54, 939-943.	2.2	43
29	Microwave resonant absorption of viruses through dipolar coupling with confined acoustic vibrations. Applied Physics Letters, 2009, 94, .	1.5	42
30	A 40-GHz Fast-Locked All-Digital Phase-Locked Loop Using a Modified Bang-Bang Algorithm. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 321-325.	2.2	42
31	A CMOS 400-Mb/s serial link for AS-memory systems using a PWM scheme. IEEE Journal of Solid-State Circuits, 2001, 36, 1498-1505.	3.5	37
32	A 3.125-Gb/s clock and data recovery circuit for the 10-Gbase-LX4 Ethernet. IEEE Journal of Solid-State Circuits, 2004, 39, 1356-1360.	3.5	37
33	All-Digital Delay-Locked Loop/Pulsewidth-Control Loop With Adjustable Duty Cycles. IEEE Journal of Solid-State Circuits, 2006, 41, 1262-1274.	3.5	37
34	A fast-lock mixed-mode DLL using a 2-b SAR algorithm. IEEE Journal of Solid-State Circuits, 2001, 36, 1464-1471.	3.5	35
35	All-Digital Fast-Locked Synchronous Duty-Cycle Corrector. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2006, 53, 1363-1367.	2.3	34
36	Analysis and Design of D-Band Injection-Locked Frequency Dividers. IEEE Journal of Solid-State Circuits, 2011, 46, 1250-1264.	3.5	34

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37	CMOS current-mode divider and its applications. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2005, 52, 145-148.	2.3	33
38	A 1.2-V 37â€“38.5-GHz Eight-Phase Clock Generator in 0.13-mum CMOS Technology. IEEE Journal of Solid-State Circuits, 2007, 42, 1261-1270.	3.5	33
39	Active-R sinusoidal oscillators using the CFA pole. International Journal of Electronics, 1994, 77, 1035-1042.	0.9	31
40	Low-power clock-deskew buffer for high-speed digital circuits. IEEE Journal of Solid-State Circuits, 1999, 34, 554-558.	3.5	30
41	A one-wire approach for skew-compensating clock distribution based on bidirectional techniques. IEEE Journal of Solid-State Circuits, 2001, 36, 266-272.	3.5	30
42	A 3.6 mW 125.7â€“131.9 GHz Divide-by-4 Injection-Locked Frequency Divider in 90 nm CMOS. IEEE Microwave and Wireless Components Letters, 2012, 22, 132-134.	2.0	30
43	A cyclic CMOS time-to-digital converter with deep sub-nanosecond resolution. , 0, , .		29
44	Systematic Generation of Current-Mode Linear Transformation Filters Based on Multiple Output CCIIs. Analog Integrated Circuits and Signal Processing, 2002, 32, 123-134.	0.9	29
45	Spur-Suppression Techniques for Frequency Synthesizers. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 653-657.	2.3	29
46	An All-Digital Fast-Locking Programmable DLL-Based Clock Generator. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 361-369.	3.5	29
47	A 0.18-$mu{hbox {m}}$ CMOS 1.25-Gbps Automatic-Gain-Control Amplifier. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 136-140.	2.2	29
48	Nanopower CMOS Relaxation Oscillators With Sub-100 <inline-formula> <tex-math notation="TeX">$hbox{ppm}/^{circ}hbox{C}$</tex-math></inline-formula> Temperature Coefficient. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 661-665.	2.2	28
49	A Subharmonically Injection-Locked PLL With Calibrated Injection Pulsewidth. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 548-552.	2.2	28
50	A double-sampling pseudo-two-path bandpass /spl Delta//spl Sigma/ modulator. IEEE Journal of Solid-State Circuits, 2000, 35, 276-280.	3.5	26
51	A Current-Reused Injection-Locked Frequency Multiplication/Division Circuit in 40-nm CMOS. IEEE Transactions on Microwave Theory and Techniques, 2013, 61, 1523-1532.	2.9	26
52	A 200-Mbps/spl sim/2-Gbps continuous-rate clock-and-data-recovery circuit. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2006, 53, 842-847.	0.1	25
53	A 104-GHz Phase-Locked Loop Using a VCO at Second Pole Frequency. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 80-88.	2.1	25
54	A Voltage Multiplier With Adaptive Threshold Voltage Compensation. IEEE Journal of Solid-State Circuits, 2017, 52, 2208-2214.	3.5	25

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55	A single-path pulsewidth control loop with a built-in delay-locked loop. IEEE Journal of Solid-State Circuits, 2005, 40, 1130-1135.	3.5	24
56	A 62.5–625-MHz Anti-Reset All-Digital Delay-Locked Loop. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 566-570.	2.3	23
57	Full-Rate Bang-Bang Phase/Frequency Detectors for Unilateral Continuous-Rate CDRs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 1214-1218.	2.2	23
58	Design of a CMOS low-power and low-voltage four-quadrant analog multiplier. Analog Integrated Circuits and Signal Processing, 2010, 63, 307-312.	0.9	23
59	New configuration for single-CCII first-order and biquadratic current-mode filters. International Journal of Electronics, 1991, 71, 637-644.	0.9	22
60	A CMOS square-law vector summation circuit. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1996, 43, 520-523.	2.3	22
61	A Low-Jitter Spread Spectrum Clock Generator Using FDMP. IEEE Transactions on Circuits and Systems II: Express Briefs, 2007, 54, 979-983.	2.2	22
62	CMOS subthreshold four-quadrant multiplier based on unbalanced source-coupled pairs. International Journal of Electronics, 1995, 78, 327-332.	0.9	21
63	A Rail-to-Rail Class-B Buffer With DC Level-Shifting Current Mirror and Distributed Miller Compensation for LCD Column Drivers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 1761-1772.	3.5	21
64	Ultrasonic Power/Data Telemetry and Neural Stimulator With OOK-PM Signaling. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 827-831.	2.2	21
65	A 20-MHz to 3-GHz Wide-Range Multiphase Delay-Locked Loop. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 850-854.	2.2	20
66	A 1â€“16-Gb/s Wide-Range Clock/Data Recovery Circuit With a Bidirectional Frequency Detector. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 487-491.	2.2	20
67	A 7.5-Gb/s One-Tap-FFE Transmitter With Adaptive Far-End Crosstalk Cancellation Using Duty Cycle Detection. IEEE Journal of Solid-State Circuits, 2013, 48, 391-404.	3.5	20
68	A Loop Gain Optimization Technique for Integer-<formula formulatype="inline"><tex Notation="TeX">N</tex></formula> TDC-Based Phase-Locked Loops. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 1873-1882.	3.5	20
69	A low-jitter and precise multiphase delay-locked loop using shifted averaging VCDL. , 0, , .		19
70	Low Jitter and Multirate Clock and Data Recovery Circuit Using a MSADLL for Chip-to-Chip Interconnection. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2004, 51, 2356-2364.	0.1	19
71	An Infinite Phase Shift Delay-Locked Loop With Voltage-Controlled Sawtooth Delay Line. IEEE Journal of Solid-State Circuits, 2008, 43, 2413-2421.	3.5	19
72	A Leakage-Compensated PLL in 65-nm CMOS Technology. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 525-529.	2.2	19

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73	A 1V 4.2mW fully integrated 2.5Gb/s CMOS limiting amplifier using folded active inductors. , 0, , .		18
74	A 20-Gb/s Transmitter With Adaptive Preemphasis in 65-nm CMOS Technology. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 319-323.	2.2	18
75	A 13.4-MHz Relaxation Oscillator With Temperature Compensation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1725-1729.	2.1	18
76	A low voltage-power 13-bit 16 MSPS CMOS pipelined ADC. IEEE Journal of Solid-State Circuits, 2004, 39, 834-836.	3.5	17
77	A 4.8-GHz Dividerless Subharmonically Injection-Locked All-Digital PLL With a FOM of $-$252.5 dB. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 547-551.	2.2	17
78	19.5 A 3.2GHz digital phase-locked loop with background supply-noise cancellation. , 2016, , .		17
79	A 2.25â€“2.7 GHz Area-Efficient Subharmonically Injection-Locked Fractional-N Frequency Synthesizer With a Fast-Converging Correlation Loop. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 811-822.	3.5	17
80	An Indoor Photovoltaic Energy Harvester Using Time-Based MPPT and On-Chip Photovoltaic Cell. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2432-2436.	2.2	17
81	A 10-MS/s-to-100-kS/s Power-Scalable Fully Differential CBSC 10-Bit Pipelined ADC With Adaptive Biasing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 11-15.	2.2	16
82	An All-Digital Jitter Tolerance Measurement Technique for CDR Circuits. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 148-152.	2.2	16
83	An 8-bit 20-MS/s ZCBC Time-Domain Analog-to-Digital Data Converter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 545-549.	2.2	15
84	A 12-bit 3.4 MS/s Two-Step Cyclic Time-Domain ADC in 0.18- CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1470-1483.	2.1	15
85	An On-Chip Relaxation Oscillator With Comparator Delay Compensation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 969-973.	2.1	15
86	CMOS oversampling Î”Î£ magnetic-to-digital converters. IEEE Journal of Solid-State Circuits, 2001, 36, 1582-1586.	3.5	14
87	A 900-MHz 1-V CMOS frequency synthesizer. IEEE Journal of Solid-State Circuits, 2000, 35, 1211-1214.	3.5	13
88	Effects of hydration levels on the bandwidth of microwave resonant absorption induced by confined acoustic vibrations. Applied Physics Letters, 2009, 95, .	1.5	13
89	A 0.43pJ/bit true random number generator. , 2014, , .		13
90	A 10-bit 40-MS/s Time-Domain Two-Step ADC With Short Calibration Time. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 126-130.	2.2	13

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91	A 0.31-pJ/bit 20-Gb/s DFE With 1 Discrete Tap and 2 IIR Filters Feedback in 40-nm-LP CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1282-1286.	2.2	13
92	An 8-bit 10 MS/s folding and interpolating ADC using the continuous-time auto-zero technique. IEEE Journal of Solid-State Circuits, 2001, 36, 122-128.	3.5	12
93	CMOS magnetic field to frequency converter. IEEE Sensors Journal, 2003, 3, 241-245.	2.4	12
94	A 1V 5-Bit 5GSample/sec CMOS ADC for UWB Receivers. , 2007, , .		12
95	A Wide-Range All-Digital Duty Cycle Corrector with a Period Monitor. , 2007, , .		12
96	A 3â€“8 GHz Delay-Locked Loop With Cycle Jitter Calibration. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 1094-1098.	2.2	12
97	A 10-Gb/s Inductorless CMOS Analog Equalizer With an Interleaved Active Feedback Topology. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 97-101.	2.2	12
98	A Digitally-Calibrated Phase-Locked Loop With Supply Sensitivity Suppression. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 592-602.	2.1	12
99	New configurations for single CCII biquads. International Journal of Electronics, 1991, 70, 609-622.	0.9	11
100	New CMOS four-quadrant multiplier and squarer circuits. Analog Integrated Circuits and Signal Processing, 1996, 9, 257.	0.9	11
101	A 1-V 10.7-MHz fourth-order bandpass /spl Delta//spl Sigma/ modulators using two switched op amps. IEEE Journal of Solid-State Circuits, 2004, 39, 2041-2045.	3.5	11
102	A Fast-Recovery Low Dropout Linear Regulator for Any-Type Output Capacitors. , 2005, , .		11
103	A 10Gbps Burst-Mode CDR Circuit in 0.18Î¼m CMOS. , 2006, , .		11
104	10-Gb/s Inductorless CDRs With Digital Frequency Calibration. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 2514-2524.	3.5	11
105	A CBSC second-order sigma-delta modulator in 3μm LTPS-TFT technology. , 2009, , .		11
106	A 10-Gb/s Adaptive Parallel Receiver With Joint XTC and DFE Using Power Detection. IEEE Journal of Solid-State Circuits, 2013, 48, 2815-2826.	3.5	11
107	A 5 Gb/s Voltage-Mode Transmitter Using Adaptive Time-Based De-Emphasis. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 959-968.	3.5	11
108	High-Q Support Transducer MEMS Resonators Enabled Low-Phase-Noise Oscillators. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, 2021, 68, 1387-1398.	1.7	11

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109	A Jitter-Tolerance-Enhanced CDR Using a GDCO-Based Phase Detector. IEEE Journal of Solid-State Circuits, 2008, 43, 1217-1226.	3.5	10
110	A 104- to 112.8-GHz CMOS Injection-Locked Frequency Divider. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 555-559.	2.2	10
111	A 1.62/2.7-Gb/s Adaptive Transmitter With Two-Tap Preemphasis Using a Propagation-Time Detector. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 178-182.	2.2	10
112	A Noise Filtering Technique for Fractional-N Frequency Synthesizers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 139-143.	2.2	10
113	A Leakage-Current-Recycling Phase-Locked Loop in 65 nm CMOS Technology. IEEE Journal of Solid-State Circuits, 2012, 47, 2693-2700.	3.5	10
114	A 2.4-GHz Area-Efficient and Fast-Locking Subharmonically Injection-Locked Type-I PLL. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2474-2478.	2.1	10
115	A 44GHz Dual-Modulus Divide-by-4/5 Prescaler in 90nm CMOS Technology. , 2006, , .		9
116	A Wide-Range PLL Using Self-Healing Prescaler/VCO in 65-nm CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 250-258.	2.1	9
117	A Time-Constant Calibrated Phase-Locked Loop With a Fast-Locked Time. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 34-37.	2.3	8
118	A 132.6-GHz Phase-Locked Loop in 65 nm Digital CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 617-621.	2.2	8
119	A 56Gbps PAM-4 optical receiver front-end. , 2017, , .		8
120	A Digital Phase-Locked Loop With Background Supply Voltage Sensitivity Minimization. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1830-1839.	3.5	8
121	Analog maximum, median and minimum circuit. , 0, , .		7
122	A Delay-Locked Loop With Statistical Background Calibration. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 961-965.	2.2	7
123	A Phase-Locked Loop With Self-Calibrated Charge Pumps in 3-$muhbox{m}$ LTPS-TFT Technology. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 142-146.	2.2	7
124	Loop latency reduction technique for all-digital clock and data recovery circuits. , 2009, , .		7
125	G-Band Injection-Locked Frequency Dividers Using pi-type LC Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 315-323.	3.5	7
126	Divide-by-Three Injection-Locked Frequency Dividers Over 200 GHz in 40-nm CMOS. IEEE Journal of Solid-State Circuits, 2013, 48, 405-416.	3.5	7

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127	A 0.035-pJ/bit/dB 20-Gb/s Adaptive Linear Equalizer With an Adaptation Time of 2.68 $muext{s}$. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 645-649.	2.2	7
128	Linear transformation all-pole filters based on current conveyors. International Journal of Electronics, 1995, 79, 439-445.	0.9	6
129	A 2.4GHz CMOS Quadrature VCO for 2.4GHz WLAN/Bluetooth Applications. , 2005, , .		6
130	A 0.1-25.5-GHz Differential Cascaded-Distributed Amplifier in 0.18- μm CMOS Technology. , 2005, , .		6
131	Selective metal parallel shunting inductor and its VCO application. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2005, 52, 1811-1818.	0.1	6
132	A DLL-Based Variable-Phase Clock Buffer. IEEE Transactions on Circuits and Systems II: Express Briefs, 2007, 54, 1072-1076.	2.2	6
133	A Single-PLL UWB Frequency Synthesizer Using Multiphase Coupled Ring Oscillator and Current-Reused Multiplier. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 107-111.	2.2	6
134	A 33.6-to-33.8 Gb/s Burst-Mode CDR in 90 nm CMOS Technology. IEEE Journal of Solid-State Circuits, 2009, 44, 775-783.	3.5	6
135	A Phase-Locked Loop With Background Leakage Current Compensation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 666-670.	2.2	6
136	3.6mW D-band divide-by-3 injection-locked frequency dividers in 65nm CMOS. , 2011, , .		6
137	A 6-GHz All-Digital Fractional-N Frequency Synthesizer Using FIR-Embedded Noise Filtering Technique. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 267-271.	2.2	6
138	A 300 GHz Divide-by-2 ILFD Using Frequency Boosting Technique. IEEE Microwave and Wireless Components Letters, 2013, 23, 599-601.	2.0	6
139	A 64-Gb/s PAM-4 Optical Receiver With Amplitude/Phase Correction and Threshold Voltage/Data Level Calibration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1726-1735.	2.1	6
140	A 0.0067-mm² 12-bit 20-MS/s SAR ADC Using Digital Place-and-Route Tools in 40-nm CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 905-914.	2.1	6
141	A 2 V clock synchronizer using digital delay-locked loop. , 0, , .		5
142	A 5Gbps CMOS Automatic Gain Control Amplifier for 10GBase-LX. , 2005, , .		5
143	A Fast Settling Low Dropout Linear Regulator with Single Miller Compensation Capacitor. , 2005, , .		5
144	A 4-54GHz Static Frequency Divider with Back-Gate Coupling. , 2007, , .		5

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145	A 2.4GHz Efficiency-Enhanced Rectifier for Wireless Telemetry. , 2007, , .		5
146	A Half-Rate Bang-Bang Phase/Frequency Detector for Continuous-Rate CDR Circuits. , 2007, , .		5
147	A 50.8â€“53-GHz Clock Generator Using a Harmonic-Locked PD in 0.13-mum CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 404-408.	2.2	5
148	An all-digital clock generator for dynamic frequency scaling. , 2009, , .		5
149	A Merged CMOS Digital Near-End Crosstalk Canceller and Analog Equalizer for Multi-Lane Serial-Link Receivers. IEEE Journal of Solid-State Circuits, 2010, 45, 433-446.	3.5	5
150	A 198.9GHz-to-201.0GHz injection-locked frequency divider in 65nm CMOS. , 2010, , .		5
151	An All-Digital Spread-Spectrum Clock Generator With Self-Calibrated Bandwidth. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 2813-2822.	3.5	5
152	A 0.3V 10bit 7.3fJ/conversion-step SAR ADC in 0.18μm CMOS. , 2014, , .		5
153	A 5-Gb/s Adaptive Digital CDR Circuit With SSC Capability and Enhanced High-Frequency Jitter Tolerance. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 161-165.	2.2	5
154	A Low-Jitter Sub-Sampling PLL With a Sub-Sampling DLL. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 269-273.	2.2	5
155	Selective metal parallel shunting inductor and its VCO application. , 0, , .		4
156	A shifted-averaging VCO with precise multiphase outputs and low jitter operation. , 0, , .		4
157	A 7-BIT 400MS/s sub-ranging flash ADC in 0.18um CMOS. , 2007, , .		4
158	A dual-band 61.4∼63GHz/75.5∼77.5GHz CMOS receiver in a 90nm technology. , 2008, , .		4
159	Frequency dividers with enhanced locking range. , 2008, , .		4
160	A delay-locked loop with digital background calibration. , 2009, , .		4
161	Decision Feedback Equalizers Using the Back-Gate Feedback Technique. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 897-901.	2.2	4
162	A digital bang-bang phase-locked loop with bandwidth calibration. , 2015, , .		4

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163	A PVT-Tolerant Injection-Locked Clock Multiplier With a Frequency Calibrator Using a Delay Time Detector. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 177-181.	2.2	4
164	A PVT-Tolerant MDLL Using a Frequency Calibrator and a Voltage Monitor. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2698-2702.	2.1	4
165	A 1.22 mW 2.4 GHz PLL Using a Single-Ring-Oscillator-Based Integrator With Background Frequency Calibration. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 2169-2179.	3.5	4
166	Electrically-programmable MOSFET-C filter. International Journal of Electronics, 1990, 68, 793-802.	0.9	3
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