Sotirios G Ziavras

List of Publications by Citations

81 papers	476 citations	11 h-index	16 g-index
102 ext. papers	594 ext. citations	2.4 avg, IF	3.69 L-index

#	Paper	IF	Citations
81	On the Characterization and Optimization of On-Chip Cache Reliability against Soft Errors. *IEEE Transactions on Computers*, **2009**, 58, 1171-1184	2.5	33
80	. *IEEE Transactions on Parallel and Distributed Systems*, **1994**, 5, 1210-1220	3.7	32
79	Parallel LU factorization of sparse matrices on FPGA-based configurable computing engines. *Concurrency Computation Practice and Experience*, **2004**, 16, 319-343	1.4	23
78	Replicating Tag Entries for Reliability Enhancement in Cache Tag Arrays. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 643-654	2.6	20
77	Parallel solution of Newton power flow equations on configurable chips. *International Journal of Electrical Power and Energy Systems*, **2007**, 29, 422-431	5.1	20
76	On the problem of expanding hypercube-based systems. *Journal of Parallel and Distributed Computing*, **1992**, 16, 41-53	4.4	17
75	Efficient hardware support for pattern matching in network intrusion detection. *Computers and Security*, **2010**, 29, 756-769	4.9	14
74	In-Register Duplication: Exploiting Narrow-Width Value for Improving Register File Reliability		13
73	Evaluating the communications capabilities of the generalized hypercube interconnection network. *Concurrency and Computation: Practice and Experience*, **1999**, 11, 281-300		13
72	Wireless sensor network-based pattern matching technique for the circumvention of environmental and stimuli-related variability in structural health monitoring. *IET Wireless Sensor Systems*, **2016**, 6, 26-33	1.6	12
71	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2009**, 17, 953-963	2.6	11
70	Novel Pipelined Architecture for Efficient Evaluation of the Square Root Using a Modified Non-Restoring Algorithm. *Journal of Signal Processing Systems*, **2012**, 67, 157-166	1.4	10
69	Self-Adaptive Data Caches for Soft-Error Reliability. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2008**, 27, 1503-1507	2.5	10
68	On the Characterization of Data Cache Vulnerability in High-Performance Embedded Microprocessors **2006**,		10
67	Multicore-based vector coprocessor sharing for performance and energy gains. *Transactions on Embedded Computing Systems*, **2013**, 13, 1-25	1.8	9
66	FPGA and ASIC square root designs for high performance and power efficiency **2013**,		9
65	Optimizing the thermal behavior of subarrayed data caches		9

64	A super-programming approach for mining association rules in parallel on PC clusters. *IEEE Transactions on Parallel and Distributed Systems*, **2004**, 15, 783-794	3.7	9
63	Pyramid mappings onto hypercubes for computer vision: Connection machine comparative study. *Concurrency and Computation: Practice and Experience*, **1993**, 5, 471-489		9
62	Runtime Partial Reconfiguration for Embedded Vector Processors **2007**,		8
61	Asymmetrically Banked Value-Aware Register Files **2007**,		8
60	FPGA implementation of a Cholesky algorithm for a shared-memory multiprocessor architecture. *International Journal of Parallel, Emergent and Distributed Systems*, **2004**, 19, 211-226		8
59	Data broadcasting and reduction, prefix computation, and sorting on reduced hypercube parallel computers. *Parallel Computing*, **1996**, 22, 595-606	1	8
58	Pipelined implementation of fixed point square root in FPGA using modified non-restoring algorithm **2010**,		7
57	Coprocessor design to support MPI primitives in configurable multiprocessors. *The Integration VLSI Journal*, **2007**, 40, 235-252	1.4	7
56	**2007**,		7
55	SCALABLE MULTIFOLDED HYPERCUBES FOR VERSATILE PARALLEL COMPUTERS. *Parallel Processing Letters*, **1995**, 05, 241-250	0.3	7
54	Low-Cost, Efficient Output-Only Infrastructure Damage Detection With Wireless Sensor Networks. *IEEE Transactions on Systems, Man, and Cybernetics: Systems*, **2020**, 50, 1003-1012	7.3	7
53	Performance-Energy Optimizations for Shared Vector Accelerators in Multicores. *IEEE Transactions on Computers*, **2015**, 64, 805-817	2.5	6
52	A Method to Measure Packet Processing Time of Hosts Using High-Speed Transmission Lines. *IEEE Systems Journal*, **2015**, 9, 1248-1251	4.3	5
51	On-chip Vector Coprocessor Sharing for Multicores **2011**,		5
50	Online Anonymity Protection in Computer-Mediated Communication. *IEEE Transactions on Information Forensics and Security*, **2010**, 5, 570-580	8	5
49	Asymmetrically banked value-aware register files for low-energy and high-performance. *Microprocessors and Microsystems*, **2008**, 32, 171-182	2.4	5
48	A Universal, Dynamically Adaptable and Programmable Network Router for Parallel Computers. *VLSI Design*, **2001**, 12, 25-52		5
47	Adaptive Multiresolution Structures for Image Processing on Parallel Computers. *Journal of Parallel and Distributed Computing*, **1994**, 23, 475-483	4.4	5

46	**2009**,		4
45	Preventing Unwanted Social Inferences with Classification Tree Analysis **2009**,		4
44	. *IEEE Transactions on Parallel and Distributed Systems*, **1993**, 4, 1230-1245	3.7	4
43	Wireless sensor network-based infrastructure damage detection constrained by energy consumption **2016**,		4
42	Resource-Driven Optimizations for Transient-Fault Detecting SuperScalar Microarchitectures. *Lecture Notes in Computer Science*, **2005**, 200-214	0.9	4
41	Re-Configurable Parallel Match Evaluators Applied to Scheduling Schemes for Input-Queued Packet Switches **2009**,		3
40	Concatenating Packets in Variable-Length Input-Queued Packet Switches with Cell-Based and Packet-Based Scheduling **2008**,		3
39	Vector Processing Support for FPGA-Oriented High Performance Applications **2007**,		3
38	FPGA-based vector processing for solving sparse sets of equations		3
37	An FPGA-Based Parallel Accelerator for Matrix Multiplications in the Newton-Raphson Method. *Lecture Notes in Computer Science*, **2005**, 458-468	0.9	3
36	**2006**,		3
35	Investigation of Various Mesh Architectures With Broadcast Buses for High-Performance Computing. *VLSI Design*, **1999**, 9, 29-54		3
34	FACILITATING HIGH-PERFORMANCE IMAGE ANALYSIS ON REDUCED HYPERCUBE (RH) PARALLEL COMPUTERS. *International Journal of Pattern Recognition and Artificial Intelligence*, **1995**, 09, 679-698	1.1	3
33	Parallel DSP algorithms on TurboNet: an experimental system with hybrid message-passing/shared-memory architecture. *Concurrency and Computation: Practice and Experience*, **1996**, 8, 387-411		3
32	Connected component labelling on the BLITZEN massively parallel processor. *Image and Vision Computing*, **1993**, 11, 665-668	3.7	3
31	Efficient infrastructure damage detection and localization using wireless sensor networks, with cluster generation for monitoring damage progression **2017**,		2
30	Modular vector processor architecture targeting at data-level parallelism. *Microprocessors and Microsystems*, **2015**, 39, 237-249	2.4	2
29	ASIC Design of Shared Vector Accelerators for Multicore Processors **2014**,		2

28	Versatile design of shared vector coprocessors for multicores. *Microprocessors and Microsystems*, **2012**, 36, 543-554	2.4	2
27	**2010**,		2
26	Hardware-Based Speed Up of Face Recognition Towards Real-Time Performance **2010**,		2
25	TRB: Tag Replication Buffer for Enhancing the Reliability of the Cache Tag Array **2010**,		2
24	BTB Access Filtering: A Low Energy and High Performance Design **2008**,		2
23	A framework for dynamic resource assignment and scheduling on reconfigurable mixed-mode on-chip multiprocessors		2
22	Dataflow computation with intelligent memories emulated on field-programmable gate arrays (FPGAs). *Microprocessors and Microsystems*, **2002**, 26, 263-280	2.4	2
21	Improved algorithms for translation of pictures represented by leaf codes. *Image and Vision Computing*, **1988**, 6, 13-20	3.7	2
20	Vector Coprocessor Virtualization for Simultaneous Multithreading. *Transactions on Embedded Computing Systems*, **2016**, 15, 1-25	1.8	2
19	Packet classification using rule caching **2013**,		1
18	Efficient structural health monitoring with wireless sensor networks using a vibration-based frequency domain pattern matching technique **2017**,		1
17	A multiprocessor-on-a-programmable-chip reconfigurable system for matrix operations with power-grid case studies. *International Journal of Computational Science and Engineering*, **2015**, 10, 181	0.4	1
16	Scheduling for input-queued packet switches by a re-configurable parallel match evaluator. *IEEE Communications Letters*, **2010**, 14, 357-359	3.8	1
15	Processor design based on dataflow concurrency. *Microprocessors and Microsystems*, **2003**, 27, 199-220	2.4	1
14	Modeling distributed data representation and its effect on parallel data accesses. *Journal of Parallel and Distributed Computing*, **2005**, 65, 1281-1289	4.4	1
13			1
12	High-performance emulation of hierarchical structures on hypercube supercomputers. *Concurrency and Computation: Practice and Experience*, **1994**, 6, 85-100		1
11	Novel FPGA-Based Signature Matching for Deep Packet Inspection. *Lecture Notes in Computer Science*, **2010**, 261-276	0.9	1

10	Exploring branch target buffer access filtering for low-energy and high-performance microarchitectures. *IET Computers and Digital Techniques*, **2012**, 6, 50	0.9	0
9	Efficient face recognition using frequency distribution curve matching. *IET Image Processing*, **2012**, 6, 1161-1169	1.7	0
8	Connection Machine results for pyramid embedding algorithms. *Lecture Notes in Computer Science*, **1992**, 31-36	0.9	0
7	Instruction Fusion for Multiscalar and Many-Core Processors. *International Journal of Parallel Programming*, **2017**, 45, 67-78	1.5	
6	Parallel generation of adaptive multiresolution structures for image processing. *Concurrency and Computation: Practice and Experience*, **1997**, 9, 241-254		
5	Robust scalability analysis and SPM case studies. *Journal of Supercomputing*, **2008**, 43, 199-223	2.5	
4	A new-generation parallel computer and its performance evaluation. *Future Generation Computer Systems*, **2000**, 17, 315-333	7.5	
3	Material identification algorithms for parallel systems. *Computers and Electrical Engineering*, **1996**, 22, 325-341	4.3	
2	Binary trees of modified hypercubes: a family of networks for hypercube-like parallel computers. *International Journal of Electronics*, **1994**, 76, 27-36	1.2	
1	FACILITATING HIGH-PERFORMANCE IMAGE ANALYSIS ON REDUCED HYPERCUBE (RH) PARALLEL COMPUTERS. *Series in Machine Perception and Artificial Intelligence*, **1995**, 23-42	0.3	