Jin-Ku Kang

List of Publications by Year
in descending order

59 papers	176 citations	1477746 6 h-index	1372195 10 g-index
59 all docs	59 docs citations	59 times ranked	130 citing authors

#	Article	IF	Citations
1	An Overhead-Reduced Key Coding Technique for High-Speed Serial Interface. IEEE Access, 2022, 10, 21187-21192.	2.6	0
2	Target Capacity Filter Pruning Method for Optimized Inference Time Based on YOLOv5 in Embedded Systems. IEEE Access, 2022, 10, 70840-70849.	2.6	3
3	A 0.32â€“2.7 Gb/s Reference-Less Continuous-Rate Clock and Data Recovery Circuit With Unrestricted and Fast Frequency Acquisition. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 2347-2351.	2.2	5
4	A Resource Efficient Integer-Arithmetic-Only FPGA-Based CNN Accelerator for Real-Time Facial Emotion Recognition. IEEE Access, 2021, 9, 104367-104381.	2.6	23
5	Adaptive Non-speculative DFE with Extended Time Constraint for PAM-4 Receiver. Journal of Semiconductor Technology and Science, 2021, 21, 166-173.	0.1	0
6	A 0.42â€“3.45 Gb/s Referenceless Clock and Data Recovery Circuit With Counter-Based Unrestricted Frequency Acquisition. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 974-978.	2.2	7
7	Eye-open monitor using two-dimensional counter value profile. IEICE Electronics Express, 2019, 16, 20190601-20190601.	0.3	1
8	Design of a third-order delta-sigma TDC with error-feedback structure. IEICE Electronics Express, 2019, 16, 20181064-20181064.	0.3	1
9	A 2.41-pJ/bit 5.4-Gb/s Dual-Loop Reference-Less CDR With Fully Digital Quarter-Rate Linear Phase Detector for Embedded DisplayPort. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2907-2920.	3.5	4
10	A Two-Step Time-to-Digital Converter using Ring Oscillator Time Amplifier. , 2018, , .		6
11	A 200 Mb/sâ¼3.2 Gb/s referenceless clock and data recovery circuit with bidirectional frequency detector. IEICE Electronics Express, 2017, 14, 20161279-20161279.	0.3	3
12	A burst-mode clock and data recovery circuit with two symmetric quadrature VCOâ€™s. IEICE Electronics Express, 2016, 13, 20161086-20161086.	0.3	1
13	A 200-Mb/s to 3-Gb/s wide-band referenceless CDR using bidirectional frequency detector. , 2016, , .		2
14	A low jitter burst-mode clock and data recovery circuit with two symmetric VCO's. , 2016, , .		0
15	On-chip jitter tolerance measurement technique with independent jitter frequency modulation from VCO in CDR. IEICE Electronics Express, 2015, 12, 20150570-20150570.	0.3	0
16	Precise time-difference repetition for TDC with delay mismatch cancelling scheme. IEICE Electronics Express, 2015, 12, 20150752-20150752.	0.3	0
17	On-chip jitter tolerance measurement technique for CDR circuits. , 2015, , .		2
18	A low power 120-to-520Mb/s clock and data recovery circuit for PWM signaling scheme. , 2015, , .		0

#	Article	IF	Citations
19	A Link Layer Design for DisplayPort Interface with State Machine Based Packet Processing. Journal of Signal Processing Systems, 2015, 79, 89-98.	1.4	1
20	Auto-delay offset cancellation technique for time difference repeating amplifier. , 2014, , .		1
21	A 2.2-mW 20â€“135-MHz False-Lock-Free DLL for Display Interface in 0.15- $muhbox{m}$ CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 554-558.	2.2	7
22	A 8.7mW 5-Gb/s clock and data recovery circuit with 0.18-µm CMOS. , 2014, , .		3
23	Avoiding noise frequency interference with binary phase pulse driving and CDS for capacitive TSP controller. IEICE Electronics Express, 2014, 11, 20140837-20140837.	0.3	3
24	A low jitter clock and data recovery with a single edge sensing Bang-Bang PD. IEICE Electronics Express, 2014, 11, 20140088-20140088.	0.3	0
25	A low-power CDR using dynamic CML latches and V/I converter merged with XOR for half-rate linear phase detection. IEICE Electronics Express, 2014, 11, 20140657-20140657.	0.3	4
26	A 1.1 mW/Gb/s 10 Gbps half-rate clock-embedded transceiver for high-speed links in 65 nm CMOS. IEICE Electronics Express, 2014, 11, 20140671-20140671.	0.3	2
27	Automatic SfM-Based 2D-to-3D Conversion for Multi-Object Scenes. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2014, E97.A, 1159-1161.	0.2	0
28	A low power BPSK demodulator for wireless implantable biomedical devices. , 2013, , .		7
29	A 5-Gb/s 11.4mW half-rate CDR in 0.18μm CMOS. , 2013, , .		0
30	An ultra-low power BPSK demodulator with dual band filtering for implantable biomedical devices. IEICE Electronics Express, 2013, 10, 20120896-20120896.	0.3	1
31	Design of Low Power Optical Channel for DisplayPort Interface. Journal of the Institute of Electronics and Information Engineers, 2013, 50, 58-63.	0.0	1
32	An audio clock regenerator with a wide dividing ratio for HDMI. , 2012, , .		2
33	A 10Gb/s adaptive equalizer with ISI level measurement. IEICE Electronics Express, 2012, 9, 1384-1390.	0.3	0
34	A 1.62/2.7/5.4Gbps clock and data recovery circuit for DisplayPort 1.2. , 2012, , .		0
35	A 60 to 200MHz SSCG with approximate Hershey-Kiss modulation profile in 0.11µm CMOS. , 2012, , .		1
36	A high-speed adaptive linear equalizer with ISI level detection using periodic training pattern. , 2012, , .		2

#	Article	IF	Citations
37	A non-coherent BPSK receiver with dual band filtering for implantable biomedical devices. , 2012, , .		1
38	Low-power non-coherent data and power recovery circuit for implantable biomedical devices. , 2011, , .		3
39	A CMOS 5.4/3.24-Gbps Dual-Rate CDR with Enhanced Quarter-Rate Linear Phase Detector. ETRI Journal, 2011, 33, 752-758.	1.2	7
40	A 4Gb/s Adaptive FFE/DFE Receiver with a Data-Dependent Jitter Measurement. IEICE Transactions on Electronics, 2011, E94-C, 1779-1786.	0.3	2
41	SSCG with Hershey-Kiss modulation profile using Dual Sigma-Delta modulators. IEICE Electronics Express, 2010, 7, 1349-1353.	0.3	6
42	A DLL-based Clock Data Recovery with a modified input format. IEICE Electronics Express, 2010, 7, 539-545.	0.3	4
43	A 1.7Gbps DLL-based Clock Data Recovery in 0.35µm CMOS. , 2010, , .		0
44	A CMOS 5.4/3.24Gbps dual-rate clock and data recovery design for DisplayPort v1.2. , 2010, , .		1
45	A 720Mbps fast auxiliary channel design for DisplayPort 1.2. , 2010, , .		0
46	A 5.4Gbps/3.24Gbps dual-rate CDR with Strengthened up/down pulse ratio. , 2009, , .		1
47	A 2.7Gbps & 1.62Gbps dual-mode clock and data recovery for DisplayPort in 0.18μm CMOS. , 2009, , .		0
48	A 5-Gb/s continuous-time adaptive equalizer and CDR using 0.18μm CMOS. , 2008, , .		1
49	A 2.7Gbps & 1.62Gbps dual-mode clock and data recovery for DisplayPort. , 2008, , .		0
50	Spread spectrum clock generator for DisplayPort. , 2008, , .		0
51	A design of DisplayPort link layer. , 2008, , .		2
52	High-speed 8B/10B encoder design using a simplified coding table. IEICE Electronics Express, 2008, 5, 581-585.	0.3	4
53	Fabrication of a 2.5GbpsÃ—4 channel optical micro-module for O-PCB application. Microelectronic Engineering, 2006, 83, 1347-1351.	1.1	28
54	2Ã— oversampling 2.5 Gbps clock and data recovery with phase picking method. Current Applied Physics, 2004, 4, 75-81.	1.1	1

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55	Self-timed pipelining using latest arriving signal detection. Electronics Letters, 2001, 37, 615.	0.5	0
56	A CMOS high-speed data recovery circuit using the matched delay sampling technique. IEEE Journal of Solid-State Circuits, 1997, 32, 1588-1596.	3.5	13
57	A CMOS adiabatic logic for low power circuit design. , 0, , .		6
58	A Clock Recovery Circuit using Half-rate 4X-Oversampling PD. , 0, , .		2
59	3.125Gbps Reference-less Clock and Data Recovery using 4X Oversampling. , 0, , .		1