

# Jorge Echavarria

## List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/4192059/publications.pdf>

Version: 2024-02-01

9  
papers

55  
citations

3311381

1  
h-index

3475538

1  
g-index

9  
all docs

9  
docs citations

9  
times ranked

36  
citing authors

| # | ARTICLE  | IF  | CITATIONS |
|---|--|-----|-----------|
| 1 | FAU: Fast and error-optimized approximate adder units on LUT-Based FPGAs. , 2016, , .  |     | 16        |
| 2 | A LUT-Based Approximate Adder. , 2016, , .   |     | 14        |
| 3 | Probabilistic Error Propagation through Approximated Boolean Networks. , 2020, , .   |     | 8         |
| 4 | Efficient Arithmetic Error Rate Calculus for Visibility Reduced Approximate Adders. IEEE Embedded Systems Letters, 2018, 10, 37-40.        | 1.9 | 6         |
| 5 | FSM merging and reduction for IP cores watermarking using Genetic Algorithms. , 2014, , .  |     | 4         |
| 6 | Can Approximate Computing Reduce Power Consumption on FPGAs?. , 2018, , .  |     | 4         |
| 7 | Self-Adaptive FPGA-Based Image Processing Filters Using Approximate Arithmetics. , 2017, , .   |     | 2         |
| 8 | AConFPGA: A Multiple-Output Boolean Function Approximation DSE Technique Targeting FPGAs. , 2018, , .                                      |     | 1         |
| 9 | Design and error analysis of accuracy-configurable sequential multipliers via segmented carry chains. IT - Information Technology, 2022, . | 0.9 | 0         |