Pieter Rombouts

List of Publications by Year
in descending order

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86	1,133	430874	434195
papers	citations	18 h-index	31 g-index

89	89	89	625
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Methodology for Readout and Ring Oscillator Optimization Toward Energy-Efficient VCO-Based ADCs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 985-998.	5.4	5
2	The Truth About 2-Level Transition Elimination in Bang-Bang PAM-4 CDRs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 469-482.	5.4	7
3	The Analog Behavior of Pseudo Digital Ring Oscillators Used in VCO ADCs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2827-2840.	5.4	20
4	A Low-Noise Instrumentation Amplifier With Built-in Anti-Aliasing for Hall Sensors. IEEE Sensors Journal, 2021, 21, 18932-18944.	4.7	5
5	Efficient Offline Outer/Inner DAC Mismatch Calibration in Wideband Î”Î£ ADCs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4259-4269.	5.4	1
6	Time-Encoding Analog-to-Digital Converters: Bridging the Analog Gap to Advanced Digital CMOS?Part 2: Architectures and Circuits. IEEE Solid-State Circuits Magazine, 2020, 12, 18-27.	0.4	15
7	Time-Encoding Analog-to-Digital Converters: Bridging the Analog Gap to Advanced Digital CMOS-Part 1: Basic Principles. IEEE Solid-State Circuits Magazine, 2020, 12, 47-55.	0.4	41
8	Enhanced circuit for linear ring VCOâ€ADCs. Electronics Letters, 2019, 55, 583-585.	1.0	16
9	VCO-ADCs with a Quadrature Band-Pass Noise-Transfer-Function. , 2019, , .		0
10	A Current-Mode Floating-Bridge Technique for Closed-Loop Î£Î” Readout of Wheatstone Bridge Sensors. , 2019, , .		0
11	Low-Pass Filtering SC-DAC for Reduced Jitter and Slewing Requirements on CTSDMs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 1369-1381.	5.4	3
12	Toward â€˜digitalâ€™ analogueâ€toâ€digital converters. Electronics Letters, 2019, 55, 568-569.	1.0	2
13	A 25 Gb/s All-Digital Clock and Data Recovery Circuit for Burst-Mode Applications in PONs. Journal of Lightwave Technology, 2018, 36, 1503-1509.	4.6	17
14	A 1.8-pJ/b, 12.5â€“25-Gb/s Wide Range All-Digital Clock and Data Recovery Circuit. IEEE Journal of Solid-State Circuits, 2018, 53, 470-483.	5.4	14
15	A Pulse Frequency Modulation Interpretation of VCOs Enabling VCO-ADC Architectures With Extended Noise Shaping. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 444-457.	5.4	51
16	Experimental results on PWM linearization of a VCO-ADC with 3rd order noise shaping. , 2018, , .		1
17	Why and How VCO-based ADCs can improve instrumentation applications. , 2018, , .		14
18	Optimal NTF zero placement in MASH VCO-ADCs with higher order noise shaping. , 2018, , .		1

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19	A Mostly Digital VCO-Based CT-SDM With Third-Order Noise Shaping. IEEE Journal of Solid-State Circuits, 2017, 52, 2141-2153.	5.4	50
20	In-line monitoring of compaction properties on a rotary tablet press during tablet manufacturing of hot-melt extruded amorphous solid dispersions. International Journal of Pharmaceutics, 2017, 517, 348-358.	5.2	24
21	Downstream processing from hot-melt extrusion towards tablets: A quality by design approach. International Journal of Pharmaceutics, 2017, 531, 235-245.	5.2	20
22	Passive Loop Filter Assistance for CTSDMs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1157-1161.	3.0	8
23	A 25 Gb/s All-Digital Clock and Data Recovery Circuit for Burst Mode Applications in PONs. , 2017, , .		0
24	Design of a lowâ€voltage opâ€ampâ€less ASDM to linearise VCOâ€ADC. Electronics Letters, 2016, 52, 911-913.	1.0	4
25	Automatic detection of oesophageal intubation based on ventilation pressure waveforms shows high sensitivity and specificity in patients with pulmonary disease. Resuscitation, 2016, 105, 36-40.	3.0	2
26	Inverse Alexander phase detector. Electronics Letters, 2016, 52, 1908-1910.	1.0	6
27	Analyzing the Effect of Clock Jitter on Self-Oscillating Sigma Delta Modulators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 200-210.	5.4	8
28	Highly linear VCO for use in VCOâ€ADCs. Electronics Letters, 2016, 52, 268-270.	1.0	57
29	True highâ€order VCOâ€based ADC. Electronics Letters, 2015, 51, 23-25.	1.0	13
30	Digital bilinear feedback for lowâ€power doubleâ€sampling sigmaâ€“delta modulators. Electronics Letters, 2015, 51, 27-29.	1.0	2
31	Influence of Jitter on Limit Cycles in Bang-Bang Clock and Data Recovery Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 1463-1471.	5.4	10
32	A 40ÂMHz-BW 12-bit continuous-time âˆ†Î£ modulator with digital calibration and 84.2ÂdB-SFDR in 90Ânm CMOS. Analog Integrated Circuits and Signal Processing, 2015, 84, 137-148.	1.4	0
33	A combined hall and stress sensor for highly accurate magnetic field sensing free from the piezo-Hall effect. , 2015, , .		0
34	Calibration of DAC Mismatch Errors in $SigmaDelta$ ADCs Based on a Sine-Wave Measurement. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 567-571.	3.0	30
35	A Describing Function Study of Saturated Quantization and Its Application to the Stability Analysis of Multi-Bit Sigma Delta Modulators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 1740-1752.	5.4	5
36	A virtually floating dual-mass accelerometer. Sensors and Actuators A: Physical, 2013, 194, 140-148.	4.1	0

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37	Method for electric field and potential calculations in Hall plates. Electronics Letters, 2013, 49, 33-34.	1.0	7
38	Analytical Expressions for the Distortion of Asynchronous Sigmaâ€“Delta Modulators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 472-476.	3.0	6
39	Continuous time modulation with PWM pre-coding and binary gm blocks. Electronics Letters, 2012, 48, 1187.	1.0	7
40	A very compact 1MS/s Nyquist-rate A/D-converter with 12 effective bits. , 2012, , .		6
41	A 8ÂmW 72ÂdB Î£Î”-modulator ADC with 2.4ÂMHz BW in 130Ânm CMOS. Analog Integrated Circuits and Signal Processing, 2012, 72, 541-548.	1.4	3
42	A selectable-bandwidth 3.5 mW, 0.03Âmm2 self-oscillating Sigma Delta modulator with 71 dB dynamic range at 5ÂMHz and 65 dB at 10ÂMHz bandwidth. Analog Integrated Circuits and Signal Processing, 2012, 72, 55-63.	1.4	3
43	Condition monitoring of laminated composite sliding bearings using embedded capacitors. Smart Materials and Structures, 2012, 21, 105022.	3.5	0
44	A 40MHz 12bit 84.2dB-SFDR continuous-time delta-sigma modulator in 90nm CMOS. , 2011, , .		6
45	A Rigorous Approach to the Robust Design of Continuous-Time $SigmaDelta$ Modulators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2829-2837.	5.4	11
46	A 5-MHz 11-Bit Self-Oscillating $SigmaDelta$ Modulator With a Delay-Based Phase Shifter in 0.025 mm^2. IEEE Journal of Solid-State Circuits, 2011, 46, 1919-1927.	5.4	19
47	Validation of Symbolic Expressions in Circuit Analysis E-Learning. IEEE Transactions on Education, 2011, 54, 564-568.	2.4	13
48	A one-path subsampling quadrature receiver based on a Î£Î” modulator with distributed resonators. Analog Integrated Circuits and Signal Processing, 2011, 68, 233-243.	1.4	0
49	A dual-mass capacitive-readout accelerometer operated near pull-in. , 2010, , .		1
50	Comments on "Performance Analysis of a Hybrid Incremental and Cyclic A/D Conversion Principle. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 1395-1395.	5.4	1
51	Simple quadrature oscillator for BIST. Electronics Letters, 2010, 46, 271.	1.0	7
52	Improved DAC driving scheme for OFDM applications. Electronics Letters, 2010, 46, 1103.	1.0	0
53	Multirate Cascaded Discrete-Time Low-Pass Î”Î£ Modulator for GSM/Bluetooth/UMTS. IEEE Journal of Solid-State Circuits, 2010, 45, 1198-1208.	5.4	43
54	Folded-cascode amplifier with efficient feedforward gain-boosting. Electronics Letters, 2010, 46, 1425.	1.0	7

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55	The Nyquist Criterion: A Useful Tool for the Robust Design of Continuous-Time $SigmaDelta$ Modulators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 416-420.	3.0	13
56	Web-Based Trainer for Electrical Circuit Analysis. IEEE Transactions on Education, 2009, 52, 185-189.	2.4	38
57	Design and implementation of a band-pass sigma delta modulator with distributed resonators. Analog Integrated Circuits and Signal Processing, 2009, 58, 243-253.	1.4	1
58	A Closed-Loop Digitally Controlled MEMS Gyroscope With Unconstrained Sigma-Delta Force-Feedback. IEEE Sensors Journal, 2009, 9, 297-305.	4.7	109
59	An Unconstrained Architecture for Systematic Design of Higher Order $SigmaDelta$ Force-Feedback Loops. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 1601-1614.	5.4	30
60	An On-Line Calibration Technique for Mismatch Errors in High-Speed DACs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 1873-1883.	5.4	8
61	Mismatch Insensitive Double-Sampling Quadrature Bandpass $SigmaDelta$ Modulation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2007, 54, 2599-2607.	5.4	18
62	Nyquist-criterion based design of a CT Î£Î”-ADC with a reduced number of comparators. , 2006, , .		1
63	Quadrature Mismatch Shaping for Digital-to-Analog Converters. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2006, 53, 2529-2538.	0.1	14
64	Quadrature Mismatch Shaping with a Complex, Data Directed Swapper. , 2006, , .		1
65	A Simple On-Chip Repetitive Sampling Setup for the Quantification of Substrate Noise. IEEE Journal of Solid-State Circuits, 2006, 41, 1062-1072.	5.4	1
66	ΣΔ ADC Design Considerations for an UMTS Receiver. , 2006, , .		3
67	A versatile Nyquist-rate A/D converter with 16â€“18 bit performance for sensor readout applications. The Integration VLSI Journal, 2005, 39, 48-61.	2.1	7
68	Improved design method for continuous-time quadrature bandpass ADCs. Electronics Letters, 2005, 41, 461.	1.0	7
69	Controlled behaviour of STF in CT modulators. Electronics Letters, 2005, 41, 896.	1.0	37
70	STF behaviour in a CT Î”Î£ modulator. , 2005, , .		1
71	Design of double-sampling /spl Sigma//spl Delta/ modulation A/D converters with bilinear integrators. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2005, 52, 715-722.	0.1	16
72	Systematic Design of Double-Sampling<tex>$SigmaDelta$</tex>A/D Converters With a Modified Noise Transfer Function. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2004, 51, 675-679.	2.2	10

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73	A Double-Sampling Extended-Counting ADC. IEEE Journal of Solid-State Circuits, 2004, 39, 411-418.	5.4	40
74	A 250-khz 94-db double-sampling Î£Î” modulation a/d converter with a modified noise transfer function. IEEE Journal of Solid-State Circuits, 2003, 38, 1657-1662.	5.4	23
75	An approach to tackle quantization noise folding in double-sampling Î£Î” modulation A/D converters. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2003, 50, 157-163.	2.2	25
76	A 13.5-b 1.2-V micropower extended counting A/D converter. IEEE Journal of Solid-State Circuits, 2001, 36, 176-183.	5.4	86
77	A study of dynamic element-matching techniques for 3-level unit elements. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2000, 47, 1177-1187.	2.2	15
78	Corrections to "A comment on 'interstage gain proration technique for digital-domain multi-step adc calibration". IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1999, 46, 1449-1449.	2.2	0
79	Corrections to "A comment on 'interstage gain proration technique for digital-domain multi-step adc calibration". IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1999, 46, 1-1.	2.2	0
80	A digital error-averaging technique for pipelined A/D conversion. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1998, 45, 1321-1323.	2.2	11
81	Linearity improvement for the switched-capacitor DAC. Electronics Letters, 1996, 32, 293.	1.0	13
82	Addressing static and dynamic errors in bandpass unit element multibit DAC's. , 0, , .		1
83	Systematic design of double-sampling Î£Î” ADC's with modified NTF. , 0, , .		1
84	Synthesis of Sigma Delta Modulators Employing Continuous Time Delays.. , 0, , .		3
85	Nyquist criterion based design of continuous time Î£Î” modulators. , 0, , .		4
86	Quadrature mismatch shaping with a complex, tree structured DAC. , 0, , .		4