Shi-Yu Huang

List of Publications by Year
in descending order

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103	1,109	623734 14	526287 27
papers	citations	h-index	g-index

104	104	104	605
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	High-Performance SIFT Hardware Accelerator for Real-Time Image Feature Extraction. IEEE Transactions on Circuits and Systems for Video Technology, 2012, 22, 340-351.	8.3	135
2	P-P-N Based 10T SRAM Cell for Low-Leakage and Resilient Subthreshold Operation. IEEE Journal of Solid-State Circuits, 2011, 46, 695-704.	5.4	120
3	Fault emulation: A new methodology for fault grading. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1999, 18, 1487-1495.	2.7	72
4	Performance Characterization of TSV in 3D IC via Sensitivity Analysis. , 2010, , .		55
5	A Low-Jitter ADPLL via a Suppressive Digital Filter and an Interpolation-Based Locking Scheme. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 165-170.	3.1	39
6	Parameterized All-Digital PLL Architecture and its Compiler to Support Easy Process Migration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 621-630.	3.1	37
7	Parametric Delay Test of Post-Bond Through-Silicon Vias in 3-D ICs via Variable Output Thresholding Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 737-747.	2.7	32
8	On improving the accuracy of multiple defect diagnosis. , 0, , .		30
9	In-Situ Method for TSV Delay Testing and Characterization Using Input Sensitivity Analysis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 443-453.	3.1	30
10	QC-Fill: Quick-and-Cool X-Filling for Multicasting-Based Scan Test. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1756-1766.	2.7	29
11	A Resilient and Power-Efficient Automatic-Power-Down Sense Amplifier for SRAM Design. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 1031-1035.	3.0	21
12	X-Calibration: A Technique for Combating Excessive Bitline Leakage Current in Nanometer SRAM Designs. IEEE Journal of Solid-State Circuits, 2008, 43, 1964-1971.	5.4	20
13	Pulse-Vanishing Test for Interposers Wires in 2.5-D IC. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1258-1268.	2.7	20
14	Quick scan chain diagnosis using signal profiling. , 0, , .		19
15	A 1.2-V 0.25-/spl mu/m clock output pixel architecture with wide dynamic range and self-offset cancellation. IEEE Sensors Journal, 2006, 6, 398-405.	4.7	18
16	The HOY Tester-Can IC Testing Go Wireless?. , 2006, , .		18
17	Delay testing and characterization of post-bond interposer wires in 2.5-D ICs. , 2013, , .		17
18	A built-in self-test and self-diagnosis scheme for heterogeneous SRAM clusters. , 0, , .		16

#	Article	IF	Citations
19	Programmable Leakage Test and Binning for TSVs With Self-Timed Timing Control. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1265-1273.	2.7	16
20	Speeding up the Byzantine fault diagnosis using symbolic simulation. , 0, , .		15
21	A 65-nm CMOS Low-Power Impulse Radar System for Human Respiratory Feature Extraction and Diagnosis on Respiratory Diseases. IEEE Transactions on Microwave Theory and Techniques, 2016, 64, 1029-1041.	4.6	15
22	Robust SRAM Design via BIST-Assisted Timing-Tracking (BATT). IEEE Journal of Solid-State Circuits, 2009, 44, 642-649.	5.4	14
23	Cloud-Based Online Ageing Monitoring for IoT Devices. IEEE Access, 2019, 7, 135964-135971.	4.2	14
24	A New Robust Paradigm for Diagnosing Hold-Time Faults in Scan Chains. , 2006, , .		12
25	Diagnosis by Image Recovery: Finding Mixed Multiple Timing Faults in a Scan Chain. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 690-694.	2.2	11
26	Built-In Speed Grading with a Process-Tolerant ADPLL. , 2007, , .		11
27	Die-to-Die Clock Synchronization for 3-D IC Using Dual Locking Mechanism. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 908-917.	5.4	11
28	A high-resolution all-digital phase-locked loop with its application to built-in speed grading for memory. , 2008, , .		10
29	Process-Resilient Low-Jitter All-Digital PLL via Smooth Code-Jumping. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 2240-2249.	3.1	10
30	Gate-delay fault diagnosis using the inject-and-evaluate paradigm. , 0, , .		9
31	Resilient Self-V$_{m DD}$-Tuning Scheme With Speed-Margining for Low-Power SRAM. IEEE Journal of Solid-State Circuits, 2009, 44, 2817-2823.	5.4	9
32	Improving scan chain diagnostic accuracy using multi-stage artificial neural networks. , 2019, , .		9
33	Time and frequency transfer system using GNSS receiver. Radio Science, 2014, 49, 1171-1182.	1.6	8
34	Nonintrusive On-Line Transition-Time Binning and Timing Failure Threat Detection for Die-to-Die Interconnects. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 2039-2048.	2.7	8
35	Cell-based delay locked loop compiler. , 2016, , .		8
36	A Ping-Pong Methodology for Boosting the Resilience of Cell-Based Delay-Locked Loop. IEEE Access, 2019, 7, 97928-97937.	4.2	8

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37	A Symbolic Inject-and-Evaluate Paradigm for Byzantine Fault Diagnosis. Journal of Electronic Testing: Theory and Applications (JETTA), 2003, 19, 161-172.	1.2	7
38	Modeling and Testing of Intra-Cell Bridging Defects Using Butterfly Structure. , 2006, , .		7
39	A unified method for parametric fault characterization of post-bond TSVs. , 2012, , .		7
40	Cloud-Based PVT Monitoring System for IoT Devices. , 2017, , .		7
41	A Low-Power SRAM Design Using Quiet-Bitline Architecture. , 0, , .		6
42	Low-cost logarithmic CMOS image sensing by nonlinear analog-to-digital conversion. IEEE Transactions on Consumer Electronics, 2005, 51, 1212-1217.	3.6	6
43	A UWB IR timed-array radar using time-shifted direct-sampling architecture. , 2012, , .		6
44	On-Line Transition-Time Monitoring for Die-to-Die Interconnects in 3D ICs. , 2014, , .		6
45	Parametric Fault Testing and Performance Characterization of Post-Bond Interposer Wires in 2.5-D ICs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 476-488.	2.7	6
46	Resilient Cell-Based Architecture for Time-to-Digital Converter. , 2017, , .		6
47	Circuit and Methodology for Testing Small Delay Faults in the Clock Network. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2087-2097.	2.7	6
48	Time-to-Digital Converter Compiler for On-Chip Instrumentation. IEEE Design and Test, 2020, 37, 101-107.	1.2	6
49	A high dynamic range CMOS image sensor design based on two-frame composition. , 0, , .		5
50	Layout-Based Defect-Driven Diagnosis for Intracell Bridging Defects. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 764-769.	2.7	5
51	DLL-Assisted Clock Synchronization Method for Multi-Die ICs. , 2017, , .		5
52	Rapid PLL Monitoring By A Novel min-MAX Time-to-Digital Converter. , 2020, , .		5
53	Diagnosis of Byzantine open-segment faults [scan testing]. , 0, , .		4
54	A fading algorithm for sequential fault diagnosis. , 0, , .		4

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55	Monitoring the delay of long interconnects via distributed TDC. , 2015, , .		4
56	Test strategies for the clock and power distribution networks in a multi-die IC. , 2017, , .		4
57	Fault and Soft Error Tolerant Delay-Locked Loop. , 2020, , .		4
58	A network security processor design based on an integrated SOC design and test platform. Proceedings - Design Automation Conference, 2006, , .	0.0	3
59	Rapid and Accurate Timing Modeling for SRAM Compiler. , 2009, , .		3
60	AF-Test: Adaptive-Frequency Scan Test Methodology for Small-Delay Defects. , 2010, , .		3
61	A high-resolution all-digital duty-cycle corrector with a new pulse-width detector. , 2010, , .		3
62	SoC power analysis framework and its application to power-thermal co-simulation. , 2011, , .		3
63	Cell-Based Process Resilient Multiphase Clock Generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 2348-2352.	3.1	3
64	Mid-bond Interposer Wire Test. , 2013, , .		3
65	A wide-range clock signal generation scheme for speed grading of a logic core. , 2016, , .		3
66	Testing of small delay faults in a clock network. , 2016, , .		3
67	The Ping-Pong Tunable Delay Line In A Super-Resilient Delay-Locked Loop. , 2019, , .		3
68	Online Safety Checking for Delay Locked Loops via Embedded Phase Error Monitor. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 735-744.	4.6	3
69	Process-Resilient Fault-Tolerant Delay-Locked Loop Using TMR With Dynamic Timing Correction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1563-1572.	2.7	3
70	Combinational circuit fault diagnosis using logic emulation. , 0, , .		2
71	A low-power SRAM for Viterbi decoder in wireless communication. IEEE Transactions on Consumer Electronics, 2008, 54, 290-295.	3.6	2
72	Split-Masking: An Output Masking Scheme for Effective Compound Defect Diagnosis in Scan Architecture With Test Compression. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 834-839.	2.7	2

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73	Programmable Leakage Test and Binning for TSVs. , 2012, , .		2
74	AC-Plus Scan Methodology for Small Delay Testing and Characterization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 329-341.	3.1	2
75	A 65nm CMOS low power impulse radar for respiratory feature extraction. , 2015, , .		2
76	Versatile Transition-Time Monitoring for Interconnects via Distributed TDC. IEEE Design and Test, 2016, 33, 23-30.	1.2	2
77	Delay Characterization and Testing of Arbitrary Multiple-Pin Interconnects. IEEE Design and Test, 2016, 33, 9-16.	1.2	2
78	Diagnosis of Intermittent Scan Chain Faults Through a Multistage Neural Network Reasoning Process. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3044-3055.	2.7	2
79	Pre-Bond and Post-Bond Testing of TSVs and Die-to-Die Interconnects. , 2016, , .		2
80	Towards the logic defect diagnosis for partial-scan designs. , 0, , .		1
81	Chip-level diagnostic strategy for full-scan designs with multiple faults. , 2003, , .		1
82	Accurate RT-level power estimation using up-down encoding. , 0, , .		1
83	ToggleFinder: accurate RTL power estimation for large designs. , 0, , .		1
84	A CMOS Micromachined Gripper Array with On-Chip Optical Detection. , 2006, , .		1
85	Accurate Whole-Chip Diagnostic Strategy for Scan Designs with Multiple Faults. Journal of Electronic Testing: Theory and Applications (JETTA), 2006, 22, 151-159.	1.2	1
86	A low-jitter all-digital phase-locked loop using a suppressive digital loop filter. , 2009, , .		1
87	On-the-fly timing-aware built-in self-repair for high-speed interposer wires in 2.5-D ICs. , 2014, , .		1
88	General Timing-Aware Built-In Self-Repair for Die-to-Die Interconnects. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1836-1846.	2.7	1
89	A Folded Locking Scheme for the Long-Range Delay Block in a Wide-Range DLL. , 2018, , .		1
90	Feedback-Bus Oscillation Ring: A General Architecture for Delay Characterization and Test of Interconnects. , 2015, , .		1

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91	On speeding up extended finite state machines using catalyst circuitry. , 0, , .		0
92	Efficient bit-oriented implementation of FIR filter using a new compressor. , 0, , .		0
93	A sizing methodology for a low-noise comparator. , 0, , .		0
94	Accurate RTL power estimation for a security processor. , 0, , .		0
95	Resilient SRAM design using BIST-assisted Timing Tracking. Memory Technology, Design and Testing (MTDT), IEEE International Workshop on, 2007, , .	0.0	0
96	Output test compression for compound defect diagnosis. , 2009, , .		0
97	Online slack-time binning for IO-registered die-to-die interconnects. , 2016, , .		0
98	Online Testing of Clock Delay Faults in a Clock Network. , 2019, , .		0
99	Tiny Phase-Error Monitor for Fault and Soft-Error-Tolerant DLL to Support Graceful Degradation and Module-Level Testing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2337-2347.	2.7	0
100	Improving the Timing of Extended Finite State Machines Via Catalyst. VLSI Design, 2002, 15, 629-635.	0.5	0
101	On-Chip Jitter Learning for PLL. IEEE Design and Test, 2021, , 1-1.	1.2	0
102	Overview of On-Chip Performance Monitors for Clock Signals. , 2020, , .		0
103	Built-In Speed Grading with a Process-Tolerant ADPLL. Proceedings of the Asian Test Symposium, 2007, , .	0.0	0