Haiwen Xu

List of Publications by Year
in descending order

14 papers	86 citations	1478505 6 h-index	1474206 9 g-index
14 all docs	14 docs citations	14 times ranked	72 citing authors

#	Article	IF	Citations
1	Monolithic Waveguide-Integrated Group IV Multiple-Quantum-Well Photodetectors on 300 mm Si Substrates. IEEE Transactions on Electron Devices, 2022, 69, 2166-2172.	3.0	4
2	Strained Silicon-on-Insulator Platform for Co-Integration of Logic and RFâ€"Part II: Comb-Like Device Architecture. IEEE Transactions on Electron Devices, 2022, 69, 1769-1775.	3.0	1
3	Highly Scaled InGaZnO Ferroelectric Field-Effect Transistors and Ternary Content-Addressable Memory. IEEE Transactions on Electron Devices, 2022, 69, 5262-5269.	3.0	13
4	Indium-Gallium-Zinc-Oxide (IGZO) Nanowire Transistors. IEEE Transactions on Electron Devices, 2021, 68, 6610-6616.	3.0	13
5	Strained Silicon-on-Insulator Platform for Cointegration of Logic and RFâ€"Part I: Implant-Induced Strain Relaxation. IEEE Transactions on Electron Devices, 2021, 68, 1425-1431.	3.0	2
6	Temperature-Dependent Operation of InGaZnO Ferroelectric Thin-Film Transistors With a Metal-Ferroelectric-Metal-Insulator- Semiconductor Structure. IEEE Electron Device Letters, 2021, 42, 1786-1789.	3.9	20
7	A Ladder Transmission Line Model for the Extraction of Ultralow Specific Contact Resistivityâ€"Part I: Theoretical Design and Simulation Study. IEEE Transactions on Electron Devices, 2020, 67, 2682-2689.	3.0	6
8	A Ladder Transmission Line Model for the Extraction of Ultralow Specific Contact Resistivityâ€"Part II: Experimental Verification. IEEE Transactions on Electron Devices, 2020, 67, 2690-2696.	3.0	4
9	Enabling UTBB Strained SOI Platform for Co-Integration of Logic and RF: Implant-Induced Strain Relaxation and Comb-Like Device Architecture. , 2020, , .		4
10	Thermal Stability and Sn Segregation of Low-Resistance Ti/p⁺-Ge_{0.95}Sn_{0.05} Contact. IEEE Electron Device Letters, 2019, 40, 1575-1578.	3.9	6
11	First Demonstration of Complementary FinFETs and Tunneling FinFETs Co-Integrated on a 200 mm GeSnOI Substrate: A Pathway towards Future Hybrid Nano-electronics Systems. , 2019, , .		4
12	A Novel Fast-Turn-Around Ladder TLM Methodology with Parasitic Metal Resistance Elimination, and 2Ã—10^{â^'10} Î©-cm²Resolution: Theoretical Design and Experimental Demonstration. , 2019, , .		0
13	Elimination of the Parasitic Metal Resistance in Transmission Line Model for Extraction of Ultralow Specific Contact Resistivity. IEEE Transactions on Electron Devices, 2019, 66, 3086-3092.	3.0	8
14	Metal/P-type GeSn Contacts with Ultra-low Specific Contact Resistivity. , 2019, , .		1