Ganesh C Patil

List of Publications by Year
in descending order

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40	244	1163117 8	1058476 14
papers	citations	h-index	g-index

40	40	40	173
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Vertical gate cavity bulk-planar junctionless FET-based biosensor for label-free detection of biomolecules. Semiconductor Science and Technology, 2022, 37, 105018.	2.0	1
2	Dielectric-Modulated Bulk-Planar Junctionless Field-Effect Transistor for Biosensing Applications. IEEE Transactions on Electron Devices, 2021, 68, 3545-3551.	3.0	15
3	Review on performance analysis of P3HT:PCBM-based bulk heterojunction organic solar cells. Semiconductor Science and Technology, 2021, 36, 045005.	2.0	36
4	Fabrication and characterization of lead sulfide and multi-walled carbon nanotube based field effect transistors using low cost chemical route. Engineering Research Express, 2021, 3, 025016.	1.6	4
5	Investigation of transport in edge passivated armchair silicene nanoribbon field effect transistor by ab-initio based Wannierised tight binding. Superlattices and Microstructures, 2021, 156, 106933.	3.1	2
6	Impact of concentration variation and thermal annealing on performance of multilayer OSC consisting of sandwiched P3HT layer between PEDOT:PSS and P3HT:PCBM. Microelectronic Engineering, 2020, 221, 111195.	2.4	11
7	Engineering substrate doping in bulk planar junctionless transistor: Scalability and variability study. Engineering Research Express, 2020, 2, 025028.	1.6	1
8	Performance Analysis of Feedback Field-Effect Transistor-Based Biosensor. IEEE Sensors Journal, 2020, 20, 13269-13276.	4.7	16
9	Performance Analysis and Thermal Reliability Study of Multilayer Organic Solar Cells. IEEE Transactions on Device and Materials Reliability, 2019, 19, 572-580.	2.0	7
10	Negative capacitance Î´â€bulk planar junctionless transistor for low power applications. Micro and Nano Letters, 2019, 14, 1107-1110.	1.3	2
11	Improving organic solar cell efficiency using solution processed poly (3â€hexylthiophene) buffer layer. Micro and Nano Letters, 2019, 14, 74-77.	1.3	6
12	Impact of Zig-Zag Layer on MoS2 based Nanoribbon Gate-all-Around Field Effect Transistor. , 2019, , .		0
13	Approach for fabricating JLT using chemically deposited cadmium sulphide and titanium dioxide. Micro and Nano Letters, 2019, 14, 1060-1063.	1.3	3
14	Thermal stability analysis of buffered layer P3HT/P3HT:PCBM organic solar cells. IET Optoelectronics, 2019, 13, 240-246.	3.3	4
15	Si ₃ N ₄ :HfO ₂ dualâ€k spacer bulk planar junctionless transistor for mixed signal integrated circuits. IET Circuits, Devices and Systems, 2019, 13, 45-50.	1.4	7
16	A Novel Channel Engineered Continuous Floating Gate MOSFET for Memory Applications. Journal of Nanoelectronics and Optoelectronics, 2019, 14, 606-613.	0.5	1
17	Analytical model for 4H-SiC superjunction drift layer with anisotropic properties for ultrahigh-voltage applications. Journal of Computational Electronics, 2017, 16, 190-201.	2.5	5
18	Dual-k HfO<inf>2</inf> Spacer Bulk Planar Junctionless Transistor for Sub-30 nm Low Power CMOS. , 2017, , .		1

#	Article	IF	Citations
19	Underlap channel silicon-on-insulator quantum dot floating-gate MOSFET for low-power memory applications. Journal of Computational Electronics, 2016, 15, 1563-1569.	2.5	5
20	Comparative analysis of partial buried oxide germanium-on-insulator p-channel MOSFETs. , 2016, , .		0
21	Novel Î´-doped partially insulated junctionless transistor for mixed signal integrated circuits. Superlattices and Microstructures, 2016, 90, 247-256.	3.1	7
22	Comparative analysis of GaN-on-3CSiC and conventional Si MOSFET for digital integrated circuits. , 2015, , .		0
23	Comparative study of Ge pMOS and In0.3Ga0.7As nMOS with Si MOSFETs for digital applications. , 2015, , .		0
24	A novel partially insulated junctionless transistor for low power nanoscale digital integrated circuits. , 2014, , .		0
25	A simple analytical model of 4H-SiC MOSFET for high temperature circuit simulations. , 2014, , .		2
26	Asymmetric drain underlap dopant-segregated Schottky barrier ultrathin-body SOI MOSFET for low-power mixed-signal circuits. Semiconductor Science and Technology, 2013, 28, 045002.	2.0	8
27	Engineering buried oxide in dopant-segregated Schottky barrier SOI MOSFET for nanoscale CMOS circuits. Microelectronics Reliability, 2013, 53, 349-355.	1.7	4
28	UTBB with ground-plane dopant-segregated schottky barrier SOI MOSFET for thermally efficient low-variability nanoscale CMOS circuits. , 2013, , .		0
29	Process and device simulations to study the impact of Ge profile of 65 nm NPN SOI HBT with buried layer. , 2013, , .		0
30	Engineering spacers in dopant-segregated Schottky barrier SOI MOSFET for nanoscale CMOS logic circuits. Semiconductor Science and Technology, 2012, 27, 045004.	2.0	19
31	A comparative study on analog/RF performance of Pt-germanide and Pt-silicide Schottky barrier pMOSFETs. , 2012, , .		1
32	Underlap channel metal source/drain SOI MOSFET for thermally efficient low-power mixed-signal circuits. Microelectronics Journal, 2012, 43, 321-328.	2.0	24
33	Impact of Segregation Layer on Scalability and Analog/RF Performance of Nanoscale Schottky Barrier SOI MOSFET. Journal of Semiconductor Technology and Science, 2012, 12, 66-74.	0.4	9
34	Si<inf>3</inf>N<inf>4</inf>: HfO<inf>2</inf> dual-k spacer dopant-segregated Schottky barrier SOI MOSFET for low-power applications. , 2011, , .		3
35	Engineering buried oxide in dopant-segregated Schottky barrier SOI MOSFET for low-variability nanoscale CMOS circuits. , 2011, , .		0
36	Asymmetric Drain Underlap Schottky Barrier SOI MOSFET for Low-Power High Performance Nanoscale CMOS Circuits. , 2011, , .		5

#	Article	IF	Citations
37	A novel Î´-doped partially insulated dopant-segregated Schottky barrier SOI MOSFET for analog/RF applications. Semiconductor Science and Technology, 2011, 26, 085002.	2.0	28
38	Scalability and RF performance of nanoscale dopant segregated Schottky barrier SOI MOSFET. , 2010, , .		4
39	A novel partially insulated Schottky source/drain MOSFET: Short channel and self heating effects. , 2010, , .		3
40	Optimisation of VCD Format and Testbench Reuse in Implementation of ASIC Tester. IETE Journal of Research, 2008, 54, 13-21.	2.6	0