Yuzhe

List of Publications by Year
in descending order

9 papers	164 citations	1478505 6 h-index	1474206 9 g-index
9 all docs	9 docs citations	9 times ranked	66 citing authors

#	Article	IF	Citations
1	Deep Learning-Driven Simultaneous Layout Decomposition and Mask Optimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 709-722.	2.7	4
2	Neural-ILT 2.0: Migrating ILT to Domain-Specific and Multitask-Enabled Neural Network. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2671-2684.	2.7	7
3	High-Speed Adder Design Space Exploration via Graph Neural Processes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2657-2670.	2.7	7
4	OpenMPL: An Open-Source Layout Decomposer. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2331-2344.	2.7	7
5	SRAF Insertion via Supervised Dictionary Learning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2849-2859.	2.7	11
6	A Unified Framework for Simultaneous Layout Decomposition and Mask Optimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 5069-5082.	2.7	5
7	GAN-OPC: Mask Optimization With Lithography-Guided Generative Adversarial Nets. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2822-2834.	2.7	42
8	Layout Hotspot Detection With Feature Tensor Generation and Deep Biased Learning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1175-1187.	2.7	63
9	Cross-Layer Optimization for High Speed Adders: A Pareto Driven Machine Learning Approach. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 2298-2311.	2.7	18