

In-Tak Cho

List of Publications by Year in Descending Order

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.

135
papers

1,378
citations

21
h-index

30
g-index

162
ext. papers

1,700
ext. citations

3.8
avg. IF

4.73
L-index

#	Paper	IF	Citations
135	Comprehensive and accurate analysis of the working principle in ferroelectric tunnel junctions using low-frequency noise spectroscopy.. <i>Nanoscale</i> , 2022 ,	7.7	6
134	Novel Dual Liner Process for Side-Shielded Forksheet Device With Superior Design Margin. <i>IEEE Transactions on Electron Devices</i> , 2022 , 1-4	2.9	
133	Effects of Postdeposition Annealing Ambience on NO ₂ Gas Sensing Performance in Si-Based FET-Type Gas Sensor. <i>IEEE Transactions on Electron Devices</i> , 2022 , 1-7	2.9	3
132	Effect of Program Error in Memristive Neural Network With Weight Quantization. <i>IEEE Transactions on Electron Devices</i> , 2022 , 1-7	2.9	2
131	Highly Efficient Self-Curing Method in MOSFET Using Parasitic Bipolar Junction Transistor. <i>IEEE Electron Device Letters</i> , 2022 , 1-1	4.4	1
130	Branched Polyethylenimine Based Field Effect Transistor for Low Humidity Detection at Room Temperature. <i>IEEE Sensors Journal</i> , 2021 , 1-1	4	1
129	CMOS-Compatible Low-Power Gated Diode Synaptic Device for Hardware-Based Neural Network. <i>IEEE Transactions on Electron Devices</i> , 2021 , 1-6	2.9	2
128	Variability of DRAM Peripheral Transistor at Liquid Nitrogen Temperature. <i>IEEE Transactions on Electron Devices</i> , 2021 , 68, 1627-1632	2.9	
127	A Systematic Compact Model Parameter Calibration with Adaptive Pattern Search Algorithm. <i>Applied Sciences (Switzerland)</i> , 2021 , 11, 4155	2.6	1
126	A Study on the Effect of the Structural Parameters and Internal Mechanism of a Bilateral Gate-Controlled S/D Symmetric and Interchangeable Bidirectional Tunnel Field Effect Transistor. <i>Nanoscale Research Letters</i> , 2021 , 16, 102	5	1
125	Novel Method Enabling Forward and Backward Propagations in NAND Flash Memory for On-Chip Learning. <i>IEEE Transactions on Electron Devices</i> , 2021 , 68, 3365-3370	2.9	1
124	FET-type gas sensors: A review. <i>Sensors and Actuators B: Chemical</i> , 2021 , 330, 129240	8.5	29
123	Double-Gated Ferroelectric-Gate Field-Effect-Transistor for Processing in Memory. <i>IEEE Electron Device Letters</i> , 2021 , 1-1	4.4	0
122	Suppression of Statistical Variability in Stacked Nanosheet Using Floating Fin Structure. <i>IEEE Electron Device Letters</i> , 2021 , 1-1	4.4	
121	Low-Latency Spiking Neural Networks Using Pre-Charged Membrane Potential and Delayed Evaluation. <i>Frontiers in Neuroscience</i> , 2021 , 15, 629000	5.1	0
120	On-chip trainable hardware-based deep Q-networks approximating a backpropagation algorithm. <i>Neural Computing and Applications</i> , 2021 , 33, 9391-9402	4.8	1
119	Response Comparison of Resistor- and Si FET-Type Gas Sensors on the Same Substrate. <i>IEEE Transactions on Electron Devices</i> , 2021 , 68, 3552-3557	2.9	0

118	Direct Gradient Calculation: Simple and Variation-Tolerant On-Chip Training Method for Neural Networks. <i>Advanced Intelligent Systems</i> , 2021 , 3, 2100064	6	0
117	Effect of Lateral Charge Diffusion on Retention Characteristics of 3D NAND Flash Cells. <i>IEEE Electron Device Letters</i> , 2021 , 42, 1148-1151	4.4	0
116	3-D AND-Type Flash Memory Architecture With High- ϵ Gate Dielectric for High-Density Synaptic Devices. <i>IEEE Transactions on Electron Devices</i> , 2021 , 68, 3801-3806	2.9	3
115	Hardware-Based Spiking Neural Networks Using Capacitor-Less Positive Feedback Neuron Devices. <i>IEEE Transactions on Electron Devices</i> , 2021 , 68, 4766-4772	2.9	
114	A novel physical unclonable function (PUF) using 16 \times 16 pure-HfO ₂ ferroelectric tunnel junction array for security applications. <i>Nanotechnology</i> , 2021 , 32,	3.4	2
113	Interlayer engineering for enhanced ferroelectric tunnel junction operations in HfO ₂ -based metal-ferroelectric-insulator-semiconductor stack. <i>Nanotechnology</i> , 2021 , 32,	3.4	4
112	Core-Shell Dual-Gate Nanowire Memory as a Synaptic Device for Neuromorphic Application. <i>IEEE Journal of the Electron Devices Society</i> , 2021 , 1-1	2.3	1
111	Effect of Word-Line Bias on Linearity of Multi-Level Conductance Steps for Multi-Layer Neural Networks Based on NAND Flash Cells. <i>Journal of Nanoscience and Nanotechnology</i> , 2020 , 20, 4138-4142	1.3	2
110	Vertical Inner Gate Transistors for 4F2 DRAM Cell. <i>IEEE Transactions on Electron Devices</i> , 2020 , 67, 944-948	4.9	3
109	Impact of the Sub-Resting Membrane Potential on Accurate Inference in Spiking Neural Networks. <i>Scientific Reports</i> , 2020 , 10, 3515	4.9	6
108	Analog Complementary Metal-Oxide-Semiconductor Integrate-and-Fire Neuron Circuit for Overflow Retaining in Hardware Spiking Neural Networks. <i>Journal of Nanoscience and Nanotechnology</i> , 2020 , 20, 3117-3122	1.3	5
107	A Simulation Study on Reducing the Grain Boundary Position Dependency in Tunneling Thin-Film Transistors Using a Wide Tunneling Area. <i>Journal of Nanoscience and Nanotechnology</i> , 2020 , 20, 6627-6631	1.3	1
106	Electrical and Thermal Performances of Omega-Shaped-Gate Nanowire Field Effect Transistors for Low Power Operation. <i>Journal of Nanoscience and Nanotechnology</i> , 2020 , 20, 4092-4096	1.3	8
105	Implementation of Synaptic Device Using Various High- ϵ Gate Dielectric Stacks. <i>Journal of Nanoscience and Nanotechnology</i> , 2020 , 20, 4292-4297	1.3	3
104	A Highly Sensitive FET-Type Humidity Sensor with Inkjet-Printed Pt-InO Nanoparticles at Room Temperature. <i>Nanoscale Research Letters</i> , 2020 , 15, 198	5	7
103	Neuromorphic Computing Using NAND Flash Memory Architecture With Pulse Width Modulation Scheme. <i>Frontiers in Neuroscience</i> , 2020 , 14, 571292	5.1	16
102	3-D Synapse Array Architecture Based on Charge-Trap Flash Memory for Neuromorphic Application. <i>Electronics (Switzerland)</i> , 2020 , 9, 57	2.6	13
101	Field Effect Transistor-Type Devices Using High- ϵ Gate Insulator Stacks for Neuromorphic Applications. <i>ACS Applied Electronic Materials</i> , 2020 , 2, 323-328	4	4

100	Pruning for Hardware-Based Deep Spiking Neural Networks Using Gated Schottky Diode as Synaptic Devices. <i>Journal of Nanoscience and Nanotechnology</i> , 2020 , 20, 6603-6608	1.3	1
99	On-Chip Training Spiking Neural Networks Using Approximated Backpropagation With Analog Synaptic Devices. <i>Frontiers in Neuroscience</i> , 2020 , 14, 423	5.1	20
98	A Novel High Schottky Barrier Based Bilateral Gate and Assistant Gate Controlled Bidirectional Tunnel Field Effect Transistor. <i>IEEE Journal of the Electron Devices Society</i> , 2020 , 8, 976-980	2.3	2
97	3D AND-Type Stacked Array for Neuromorphic Systems. <i>Micromachines</i> , 2020 , 11,	3.3	2
96	A Spiking Neural Network with a Global Self-Controller for Unsupervised Learning Based on Spike-Timing-Dependent Plasticity Using Flash Memory Synaptic Devices 2019 ,		5
95	Characterization of a Capacitorless DRAM Cell for Cryogenic Memory Applications. <i>IEEE Electron Device Letters</i> , 2019 , 40, 1614-1617	4.4	5
94	A polycrystalline-silicon dual-gate MOSFET-based 1T-DRAM using grain boundary-induced variable resistance. <i>Applied Physics Letters</i> , 2019 , 114, 183503	3.4	10
93	Low-Frequency Noise Characteristics in Multi-Layer WSe ₂ Field Effect Transistors with Different Contact Metals. <i>Journal of Nanoscience and Nanotechnology</i> , 2019 , 19, 6422-6428	1.3	2
92	Humidity-Sensitive Field Effect Transistor with In ₂ O ₃ Nanoparticles as a Sensing Layer. <i>Journal of Nanoscience and Nanotechnology</i> , 2019 , 19, 6656-6662	1.3	8
91	Gated Schottky Diode-Type Synaptic Device with a Field-Plate Structure to Reduce the Forward Current. <i>Journal of Nanoscience and Nanotechnology</i> , 2019 , 19, 6135-6138	1.3	
90	Design Optimization and Analysis of InGaAs/InAs/InGaAs Heterojunction-Based Electron Hole Bilayer Tunneling FETs. <i>Journal of Nanoscience and Nanotechnology</i> , 2019 , 19, 6070-6076	1.3	2
89	Fabrication and Characterization of a Thin-Body Poly-Si 1T DRAM With Charge-Trap Effect. <i>IEEE Electron Device Letters</i> , 2019 , 40, 566-569	4.4	15
88	Field-Effect Transistors: Threshold Voltage Control of Multilayered MoS ₂ Field-Effect Transistors via Octadecyltrichlorosilane and their Applications to Active Matrixed Quantum Dot Displays Driven by Enhancement-Mode Logic Gates (Small 7/2019). <i>Small</i> , 2019 , 15, 1970037	11	
87	Adaptive learning rule for hardware-based deep neural networks using electronic synapse devices. <i>Neural Computing and Applications</i> , 2019 , 31, 8101-8116	4.8	29
86	Analysis on New Read Disturbance Induced by Hot Carrier Injections in 3-D Channel-Stacked NAND Flash Memory. <i>IEEE Transactions on Electron Devices</i> , 2019 , 66, 3326-3330	2.9	3
85	Synaptic Devices Based on 3-D AND Flash Memory Architecture for Neuromorphic Computing 2019 ,		7
84	Grayscale Image Recognition Using Spike-Rate-Based Online Learning and Threshold Adjustment of Neurons in a Thin-Film Transistor-Type NOR Flash Memory Array. <i>Journal of Nanoscience and Nanotechnology</i> , 2019 , 19, 6055-6060	1.3	2
83	Unsupervised Online Learning With Multiple Postsynaptic Neurons Based on Spike-Timing-Dependent Plasticity Using a Thin-Film Transistor-Type NOR Flash Memory Array. <i>Journal of Nanoscience and Nanotechnology</i> , 2019 , 19, 6050-6054	1.3	7

82	Reconfigurable Field-Effect Transistor as a Synaptic Device for XNOR Binary Neural Network. <i>IEEE Electron Device Letters</i> , 2019 , 40, 624-627	4.4	13
81	Accurate identification of gas type and concentration using DNN reflecting the sensing properties of MOSFET-type gas sensor 2019 ,		4
80	Investigation on Ambipolar Current Suppression Using a Stacked Gate in an L-shaped Tunnel Field-Effect Transistor. <i>Micromachines</i> , 2019 , 10,	3.3	3
79	Review of candidate devices for neuromorphic applications 2019 ,		1
78	Threshold Voltage Control of Multilayered MoS Field-Effect Transistors via Octadecyltrichlorosilane and their Applications to Active Matrixed Quantum Dot Displays Driven by Enhancement-Mode Logic Gates. <i>Small</i> , 2019 , 15, e1803852	11	14
77	3-D Stacked Synapse Array Based on Charge-Trap Flash Memory for Implementation of Deep Neural Networks. <i>IEEE Transactions on Electron Devices</i> , 2019 , 66, 420-427	2.9	22
76	Scaling Effect on Silicon Nitride Memristor with Highly Doped Si Substrate. <i>Small</i> , 2018 , 14, e1704062	11	55
75	Novel Boosting Scheme Using Asymmetric Pass Voltage for Reducing Program Disturbance in 3-Dimensional NAND Flash Memory. <i>IEEE Journal of the Electron Devices Society</i> , 2018 , 1-1	2.3	3
74	Demonstration of Unsupervised Learning With Spike-Timing-Dependent Plasticity Using a TFT-Type NOR Flash Memory Array. <i>IEEE Transactions on Electron Devices</i> , 2018 , 65, 1774-1780	2.9	40
73	Spiking Neural Network Using Synaptic Transistors and Neuron Circuits for Pattern Recognition With Noisy Images. <i>IEEE Electron Device Letters</i> , 2018 , 39, 630-633	4.4	42
72	Reconfigurable Cell String Having FET and Super-Steep Switching Diode Operation in 3D NAND Flash Memory 2018 ,		2
71	Hardware-based Neural Networks using a Gated Schottky Diode as a Synapse Device 2018 ,		9
70	Graphene electrode with tunable charge transport in thin-film transistors. <i>Nano Research</i> , 2018 , 11, 274-286	2.86	14
69	A Split-Gate Positive Feedback Device With an Integrate-and-Fire Capability for a High-Density Low-Power Neuron Circuit. <i>Frontiers in Neuroscience</i> , 2018 , 12, 704	5.1	10
68	A source drain symmetric and interchangeable bidirectional tunneling field effect transistor. <i>AIP Advances</i> , 2018 , 8, 085318	1.5	1
67	1/f-Noise in AlGaIn/GaN Nanowire Omega-FinFETs. <i>IEEE Electron Device Letters</i> , 2017 , 38, 252-254	4.4	17
66	High-Density Reconfigurable Devices With Programmable Bottom-Gate Array. <i>IEEE Electron Device Letters</i> , 2017 , 38, 564-567	4.4	8
65	A novel high-performance H-gate U-channel junctionless FET. <i>Journal of Computational Electronics</i> , 2017 , 16, 287-295	1.8	2

64	Pulse Biasing Scheme for the Fast Recovery of FET-Type Gas Sensors for Reducing Gases. <i>IEEE Electron Device Letters</i> , 2017 , 38, 971-974	4.4	8
63	Analysis of Clockwise and Counter-Clockwise Hysteresis Characteristics in 3-D NAND Flash Memory Cells. <i>IEEE Electron Device Letters</i> , 2017 , 38, 867-870	4.4	2
62	High-Density and Near-Linear Synaptic Device Based on a Reconfigurable Gated Schottky Diode. <i>IEEE Electron Device Letters</i> , 2017 , 38, 1153-1156	4.4	38
61	A 650 V Super-Junction MOSFET With Novel Hexagonal Structure for Superior Static Performance and High BV Resilience to Charge Imbalance: A TCAD Simulation Study. <i>IEEE Electron Device Letters</i> , 2017 , 38, 111-114	4.4	18
60	Ultralow power switching in a silicon-rich SiN/SiN double-layer resistive memory device. <i>Physical Chemistry Chemical Physics</i> , 2017 , 19, 18988-18995	3.6	25
59	Design Consideration of Diode-Type NAND Flash Memory Cell String Having Super-Steep Switching Slope. <i>IEEE Journal of the Electron Devices Society</i> , 2016 , 4, 328-334	2.3	2
58	Elimination of the gate and drain bias stresses in I_V characteristics of WSe ₂ FETs by using dual channel pulse measurement. <i>Applied Physics Letters</i> , 2016 , 109, 053503	3.4	7
57	Accurate extraction of WSe ₂ FETs parameters by using pulsed I-V method at various temperatures. <i>Nano Convergence</i> , 2016 , 3, 31	9.2	4
56	Layer Selection by Multi-Level Permutation in 3-D Stacked NAND Flash Memory. <i>IEEE Electron Device Letters</i> , 2016 , 37, 866-869	4.4	3
55	Optimization of saddle junctionless FETs for extreme high integration. <i>Journal of Computational Electronics</i> , 2016 , 15, 801-808	1.8	3
54	Negligible hysteresis of molybdenum disulfide field-effect transistors through thermal annealing. <i>Journal of Information Display</i> , 2016 , 17, 103-108	4.1	8
53	Analysis on Program Disturbance in Channel-Stacked NAND Flash Memory With Layer Selection by Multilevel Operation. <i>IEEE Transactions on Electron Devices</i> , 2016 , 63, 1041-1046	2.9	11
52	Silicon-Based Floating-Body Synaptic Transistor With Frequency-Dependent Short- and Long-Term Memories. <i>IEEE Electron Device Letters</i> , 2016 , 37, 249-252	4.4	52
51	Novel Program Method of String Select Transistors for Layer Selection in Channel-Stacked NAND Flash Memory. <i>IEEE Transactions on Electron Devices</i> , 2016 , 63, 3521-3526	2.9	2
50	Trap Profiling in Nitride Storage Layer in 3-D NAND Flash Memory Using Retention Characteristics and AC- g_{m} Method. <i>IEEE Electron Device Letters</i> , 2015 , 36, 561-563	4.4	3
49	Water-soluble thin film transistors and circuits based on amorphous indium-gallium-zinc oxide. <i>ACS Applied Materials & Interfaces</i> , 2015 , 7, 8268-74	9.5	98
48	A novel high performance junctionless FETs with saddle-gate. <i>Journal of Computational Electronics</i> , 2015 , 14, 661-668	1.8	8
47	Implementation of Short-Term Plasticity and Long-Term Potentiation in a Synapse Using Si-Based Type of Charge-Trap Memory. <i>IEEE Transactions on Electron Devices</i> , 2015 , 62, 569-573	2.9	21

46	Effectiveness of a Guard Ring Utilizing an Inversion Layer Surrounding a Through Silicon Via. <i>IEEE Electron Device Letters</i> , 2015 , 36, 268-270	4.4	4
45	Low frequency noise characteristics in multilayer WSe ₂ field effect transistor. <i>Applied Physics Letters</i> , 2015 , 106, 023504	3.4	23
44	GIDL Characteristics in Gated-Diode Memory String and Its Application to Current-Steering Digital-to-Analog Conversion. <i>IEEE Transactions on Electron Devices</i> , 2015 , 62, 3272-3277	2.9	4
43	Analysis and suppression of drain current drift in graphene FETs. <i>Semiconductor Science and Technology</i> , 2015 , 30, 105013	1.8	1
42	Fluorinated CYTOP passivation effects on the electrical reliability of multilayer MoS ₂ field-effect transistors. <i>Nanotechnology</i> , 2015 , 26, 455201	3.4	34
41	Extraction of Interface Trap Density in the Region Between Adjacent Wordlines in NAND Flash Memory Strings. <i>IEEE Electron Device Letters</i> , 2015 , 36, 53-55	4.4	1
40	Low-Frequency Noise Properties in Double-Gate Amorphous InGaZnO Thin-Film Transistors Fabricated by Back-Channel-Etch Method. <i>IEEE Electron Device Letters</i> , 2015 , 36, 1332-1335	4.4	15
39	Local-Degradation-Induced Threshold Voltage Shift in Turned-OFF Amorphous InGaZnO Thin Film Transistors Under AC Drain Bias Stress. <i>IEEE Electron Device Letters</i> , 2015 , 36, 579-581	4.4	11
38	Simulation study on deep nanoscale short channel junctionless SOI FinFETs with triple-gate or double-gate structures. <i>Journal of Computational Electronics</i> , 2014 , 13, 509-514	1.8	18
37	Effect of Temperature and Electric Field on Degradation in Amorphous InGaZnO TFTs Under Positive Gate and Drain Bias Stress. <i>IEEE Electron Device Letters</i> , 2014 , 35, 458-460	4.4	23
36	Fundamental effects in nanoscale thermocapillary flow. <i>Journal of Applied Physics</i> , 2014 , 115, 054315	2.5	8
35	Effects of the active layers deposition temperature on the electrical performance of p-type SnO thin-film Transistors. <i>Journal of the Korean Physical Society</i> , 2014 , 65, 286-290	0.6	7
34	Microwave purification of large-area horizontally aligned arrays of single-walled carbon nanotubes. <i>Nature Communications</i> , 2014 , 5, 5332	17.4	37
33	Improvement of Long-Term Durability and Bias Stress Stability in p-Type SnO Thin-Film Transistors Using a SU-8 Passivation Layer. <i>IEEE Electron Device Letters</i> , 2014 , 35, 1260-1262	4.4	41
32	Switching and conduction mechanism of Cu/Si ₃ N ₄ /Si RRAM with CMOS compatibility 2014 ,		2
31	Pulsed I _{ds} measurement method to obtain hysteresis-free characteristics of graphene FETs. <i>Semiconductor Science and Technology</i> , 2014 , 29, 095006	1.8	4
30	Suppression of Read Disturb Fail Caused by Boosting Hot Carrier Injection Effect for 3-D Stack NAND Flash Memories. <i>IEEE Electron Device Letters</i> , 2014 , 35, 42-44	4.4	13
29	Border trap characterization in amorphous indium-gallium-zinc oxide thin-film transistors with SiO _x and SiN _x gate dielectrics. <i>Applied Physics Letters</i> , 2013 , 103, 142104	3.4	12

28	Investigation of the charge transport mechanism and subgap density of states in p-type Cu ₂ O thin-film transistors. <i>Applied Physics Letters</i> , 2013 , 102, 082103	3-4	32
27	Flicker Noise Behavior in Resistive Memory Devices With Double-Layered Transition Metal Oxide. <i>IEEE Electron Device Letters</i> , 2013 , 34, 244-246	4-4	3
26	Bias-Stress-Induced Instabilities in P-Type Cu_2O Thin-Film Transistors. <i>IEEE Electron Device Letters</i> , 2013 , 34, 647-649	4-4	20
25	L-Shaped Tunneling Field-Effect Transistors for Complementary Logic Applications. <i>IEICE Transactions on Electronics</i> , 2013 , E96.C, 634-638	0-4	1
24	Relationship Between Conduction Mechanism and Low-Frequency Noise in Polycrystalline- TiO_x -Based Resistive-Switching Memory Devices. <i>IEEE Electron Device Letters</i> , 2012 , 33, 1063-1065	4-4	3
23	Extraction of the Channel Mobility in InGaZnO TFTs Using Multifrequency Capacitance-Voltage Method. <i>IEEE Electron Device Letters</i> , 2012 , 33, 815-817	4-4	4
22	Characteristics of Elliptical Gate-All-Around SONOS Nanowire With Effective Circular Radius. <i>IEEE Electron Device Letters</i> , 2012 , 33, 1613-1615	4-4	2
21	Poly-silicon quantum-dot single-electron transistors. <i>Journal of the Korean Physical Society</i> , 2012 , 60, 108-112	0-6	1
20	Effect of Temperature and Humidity on NO_2 and NH_3 Gas Sensitivity of Bottom-Gate Graphene FETs Prepared by ICP-CVD. <i>IEEE Electron Device Letters</i> , 2012 , 33, 1084-1086	4-4	27
19	New Read Schemes Using Boosted Channel Potential of Adjacent Bit-Line Strings in nand Flash Memory. <i>IEEE Electron Device Letters</i> , 2012 , 33, 1198-1200	4-4	2
18	Threshold Voltage Fluctuation by Random Telegraph Noise in Floating Gate nand Flash Memory String. <i>IEEE Transactions on Electron Devices</i> , 2011 , 58, 67-73	2-9	29
17	High-Density Three-Dimensional Stacked nand Flash With Common Gate Structure and Shield Layer. <i>IEEE Transactions on Electron Devices</i> , 2011 , 58, 4212-4218	2-9	4
16	Single-Crystalline Si Stacked ARray (STAR) NAND Flash Memory. <i>IEEE Transactions on Electron Devices</i> , 2011 , 58, 1006-1014	2-9	21
15	Non-ideal characteristic analysis of GaN-based light-emitting diode using current-voltage (I-V) and low-frequency noise experiment 2011 ,		1
14	Investigation of Gate Etch Damage at Metal/High- κ Gate Dielectric Stack Through Random Telegraph Noise in Gate Edge Direct Tunneling Current. <i>IEEE Electron Device Letters</i> , 2011 , 32, 569-571	4-4	13
13	Accurate extraction of I/I due to random telegraph noise in gate edge current of high- κ n-type metal-oxide-semiconductor field-effect transistors under accumulation mode. <i>Applied Physics Letters</i> , 2011 , 98, 023505	3-4	3
12	Electrical instabilities and low-frequency noise in InGaZnO thin film transistors 2010 ,		2
11	Novel Double-Gate 1T-DRAM Cell Using Nonvolatile Memory Functionality for High-Performance and Highly Scalable Embedded DRAMs. <i>IEEE Transactions on Electron Devices</i> , 2010 , 57, 614-619	2-9	6

10	Investigation of Random Telegraph Noise in Gate-Induced Drain Leakage and Gate Edge Direct Tunneling Currents of High- κ MOSFETs. <i>IEEE Transactions on Electron Devices</i> , 2010 , 57, 913-918	2.9	19
9	Observation of Slow Oxide Traps at MOSFETs Having Metal/High-k Gate Dielectric Stack in Accumulation Mode. <i>IEEE Transactions on Electron Devices</i> , 2010 , 57, 2697-2703	2.9	7
8	Study of Si implantation into Mg-doped GaN for MOSFETs. <i>Physica Status Solidi C: Current Topics in Solid State Physics</i> , 2010 , 7, 1964-1966		3
7	Detection of Interleaved OFDMA Uplink Signals in the Presence of Residual Frequency Offset Using the SAGE Algorithm. <i>IEEE Transactions on Vehicular Technology</i> , 2007 , 56, 1455-1460	6.8	8
6	Time and Frequency Synchronization for OFDMA Uplink System using the SAGE Algorithm. <i>IEEE Transactions on Wireless Communications</i> , 2007 , 6, 1176-1181	9.6	19
5	Joint carrier frequency synchronization and channel estimation for OFDM systems via the EM algorithm. <i>IEEE Transactions on Vehicular Technology</i> , 2006 , 55, 167-172	6.8	40
4	Joint Common Phase Error and Channel Estimation for OFDM-based WLANs in the Presence of Wiener Phase Noise and Residual Frequency Offset 2006 ,		2
3	Channel optimized predistortion for self-heterodyne DCT-based OFDM systems. <i>IEEE Transactions on Consumer Electronics</i> , 2005 , 51, 770-775	4.8	1
2	Electrical characteristics of FinFET with vertically nonuniform source/drain doping profile. <i>IEEE Nanotechnology Magazine</i> , 2002 , 1, 233-237	2.6	18
1	Joint channel estimation and phase noise suppression for OFDM systems		1