# In-Tak Cho

## List of Publications by Citations



| | | | |
|---|---|---|---|
| 135 papers | 1,378 citations | 21 h-index | 30 g-index |
| 162 ext. papers | 1,700 ext. citations | 3.8 avg, IF | 4.73 L-index |

| # | Paper | IF | Citations |
|---|---|---|---|
| 135 | Water-soluble thin film transistors and circuits based on amorphous indium-gallium-zinc oxide. *ACS Applied Materials & Interfaces*, **2015**, 7, 8268-74 | 9.5 | 98 |
| 134 | Scaling Effect on Silicon Nitride Memristor with Highly Doped Si Substrate. *Small*, **2018**, 14, e1704062 | 11 | 55 |
| 133 | Silicon-Based Floating-Body Synaptic Transistor With Frequency-Dependent Short- and Long-Term Memories. *IEEE Electron Device Letters*, **2016**, 37, 249-252 | 4.4 | 52 |
| 132 | Spiking Neural Network Using Synaptic Transistors and Neuron Circuits for Pattern Recognition With Noisy Images. *IEEE Electron Device Letters*, **2018**, 39, 630-633 | 4.4 | 42 |
| 131 | Improvement of Long-Term Durability and Bias Stress Stability in p-Type SnO Thin-Film Transistors Using a SU-8 Passivation Layer. *IEEE Electron Device Letters*, **2014**, 35, 1260-1262 | 4.4 | 41 |
| 130 | Demonstration of Unsupervised Learning With Spike-Timing-Dependent Plasticity Using a TFT-Type NOR Flash Memory Array. *IEEE Transactions on Electron Devices*, **2018**, 65, 1774-1780 | 2.9 | 40 |
| 129 | Joint carrier frequency synchronization and channel estimation for OFDM systems via the EM algorithm. *IEEE Transactions on Vehicular Technology*, **2006**, 55, 167-172 | 6.8 | 40 |
| 128 | High-Density and Near-Linear Synaptic Device Based on a Reconfigurable Gated Schottky Diode. *IEEE Electron Device Letters*, **2017**, 38, 1153-1156 | 4.4 | 38 |
| 127 | Microwave purification of large-area horizontally aligned arrays of single-walled carbon nanotubes. *Nature Communications*, **2014**, 5, 5332 | 17.4 | 37 |
| 126 | Fluorinated CYTOP passivation effects on the electrical reliability of multilayer MoS□ field-effect transistors. *Nanotechnology*, **2015**, 26, 455201 | 3.4 | 34 |
| 125 | Investigation of the charge transport mechanism and subgap density of states in p-type Cu2O thin-film transistors. *Applied Physics Letters*, **2013**, 102, 082103 | 3.4 | 32 |
| 124 | Adaptive learning rule for hardware-based deep neural networks using electronic synapse devices. *Neural Computing and Applications*, **2019**, 31, 8101-8116 | 4.8 | 29 |
| 123 | Threshold Voltage Fluctuation by Random Telegraph Noise in Floating Gate nand Flash Memory String. *IEEE Transactions on Electron Devices*, **2011**, 58, 67-73 | 2.9 | 29 |
| 122 | FET-type gas sensors: A review. *Sensors and Actuators B: Chemical*, **2021**, 330, 129240 | 8.5 | 29 |
| 121 | Effect of Temperature and Humidity on $hbox{NO}_{2}$ and $hbox{NH}_{3}$ Gas Sensitivity of Bottom-Gate Graphene FETs Prepared by ICP-CVD. *IEEE Electron Device Letters*, **2012**, 33, 1084-1086 | 4.4 | 27 |
| 120 | Ultralow power switching in a silicon-rich SiN/SiN double-layer resistive memory device. *Physical Chemistry Chemical Physics*, **2017**, 19, 18988-18995 | 3.6 | 25 |
| 119 | Low frequency noise characteristics in multilayer WSe2 field effect transistor. *Applied Physics Letters*, **2015**, 106, 023504 | 3.4 | 23 |

| | | | |
|---|---|---|---|
| 118 | Effect of Temperature and Electric Field on Degradation in Amorphous InGaZnO TFTs Under Positive Gate and Drain Bias Stress. *IEEE Electron Device Letters*, **2014**, 35, 458-460 | 4.4 | 23 |
| 117 | 3-D Stacked Synapse Array Based on Charge-Trap Flash Memory for Implementation of Deep Neural Networks. *IEEE Transactions on Electron Devices*, **2019**, 66, 420-427 | 2.9 | 22 |
| 116 | Implementation of Short-Term Plasticity and Long-Term Potentiation in a Synapse Using Si-Based Type of Charge-Trap Memory. *IEEE Transactions on Electron Devices*, **2015**, 62, 569-573 | 2.9 | 21 |
| 115 | Single-Crystalline Si STacked ARray (STAR) NAND Flash Memory. *IEEE Transactions on Electron Devices*, **2011**, 58, 1006-1014 | 2.9 | 21 |
| 114 | Bias-Stress-Induced Instabilities in P-Type ${rm Cu}_{2}{rm O}$ Thin-Film Transistors. *IEEE Electron Device Letters*, **2013**, 34, 647-649 | 4.4 | 20 |
| 113 | On-Chip Training Spiking Neural Networks Using Approximated Backpropagation With Analog Synaptic Devices. *Frontiers in Neuroscience*, **2020**, 14, 423 | 5.1 | 20 |
| 112 | Investigation of Random Telegraph Noise in Gate-Induced Drain Leakage and Gate Edge Direct Tunneling Currents of High-$k$ MOSFETs. *IEEE Transactions on Electron Devices*, **2010**, 57, 913-918 | 2.9 | 19 |
| 111 | Time and Frequency Synchronization for OFDMA Uplink System using the SAGE Algorithm. *IEEE Transactions on Wireless Communications*, **2007**, 6, 1176-1181 | 9.6 | 19 |
| 110 | A 650 V Super-Junction MOSFET With Novel Hexagonal Structure for Superior Static Performance and High BV Resilience to Charge Imbalance: A TCAD Simulation Study. *IEEE Electron Device Letters*, **2017**, 38, 111-114 | 4.4 | 18 |
| 109 | Simulation study on deep nanoscale short channel junctionless SOI FinFETs with triple-gate or double-gate structures. *Journal of Computational Electronics*, **2014**, 13, 509-514 | 1.8 | 18 |
| 108 | Electrical characteristics of FinFET with vertically nonuniform source/drain doping profile. *IEEE Nanotechnology Magazine*, **2002**, 1, 233-237 | 2.6 | 18 |
| 107 | 1/f-Noise in AlGaN/GaN Nanowire Omega-FinFETs. *IEEE Electron Device Letters*, **2017**, 38, 252-254 | 4.4 | 17 |
| 106 | Neuromorphic Computing Using NAND Flash Memory Architecture With Pulse Width Modulation Scheme. *Frontiers in Neuroscience*, **2020**, 14, 571292 | 5.1 | 16 |
| 105 | Fabrication and Characterization of a Thin-Body Poly-Si 1T DRAM With Charge-Trap Effect. *IEEE Electron Device Letters*, **2019**, 40, 566-569 | 4.4 | 15 |
| 104 | Low-Frequency Noise Properties in Double-Gate Amorphous InGaZnO Thin-Film Transistors Fabricated by Back-Channel-Etch Method. *IEEE Electron Device Letters*, **2015**, 36, 1332-1335 | 4.4 | 15 |
| 103 | Threshold Voltage Control of Multilayered MoS Field-Effect Transistors via Octadecyltrichlorosilane and their Applications to Active Matrixed Quantum Dot Displays Driven by Enhancement-Mode Logic Gates. *Small*, **2019**, 15, e1803852 | 11 | 14 |
| 102 | Graphene electrode with tunable charge transport in thin-film transistors. *Nano Research*, **2018**, 11, 274-286 | 10 | 14 |
| 101 | Suppression of Read Disturb Fail Caused by Boosting Hot Carrier Injection Effect for 3-D Stack NAND Flash Memories. *IEEE Electron Device Letters*, **2014**, 35, 42-44 | 4.4 | 13 |

| | | | |
|---|---|---|---|
| 100 | Investigation of Gate Etch Damage at Metal/High-$k$ Gate Dielectric Stack Through Random Telegraph Noise in Gate Edge Direct Tunneling Current. *IEEE Electron Device Letters*, **2011**, 32, 569-571 | 4.4 | 13 |
| 99 | 3-D Synapse Array Architecture Based on Charge-Trap Flash Memory for Neuromorphic Application. *Electronics (Switzerland)*, **2020**, 9, 57 | 2.6 | 13 |
| 98 | Reconfigurable Field-Effect Transistor as a Synaptic Device for XNOR Binary Neural Network. *IEEE Electron Device Letters*, **2019**, 40, 624-627 | 4.4 | 13 |
| 97 | Border trap characterization in amorphous indium-gallium-zinc oxide thin-film transistors with SiOX and SiNX gate dielectrics. *Applied Physics Letters*, **2013**, 103, 142104 | 3.4 | 12 |
| 96 | Analysis on Program Disturbance in Channel-Stacked NAND Flash Memory With Layer Selection by Multilevel Operation. *IEEE Transactions on Electron Devices*, **2016**, 63, 1041-1046 | 2.9 | 11 |
| 95 | Local-Degradation-Induced Threshold Voltage Shift in Turned-OFF Amorphous InGaZnO Thin Film Transistors Under AC Drain Bias Stress. *IEEE Electron Device Letters*, **2015**, 36, 579-581 | 4.4 | 11 |
| 94 | A polycrystalline-silicon dual-gate MOSFET-based 1T-DRAM using grain boundary-induced variable resistance. *Applied Physics Letters*, **2019**, 114, 183503 | 3.4 | 10 |
| 93 | A Split-Gate Positive Feedback Device With an Integrate-and-Fire Capability for a High-Density Low-Power Neuron Circuit. *Frontiers in Neuroscience*, **2018**, 12, 704 | 5.1 | 10 |
| 92 | Hardware-based Neural Networks using a Gated Schottky Diode as a Synapse Device **2018**, | | 9 |
| 91 | High-Density Reconfigurable Devices With Programmable Bottom-Gate Array. *IEEE Electron Device Letters*, **2017**, 38, 564-567 | 4.4 | 8 |
| 90 | Pulse Biasing Scheme for the Fast Recovery of FET-Type Gas Sensors for Reducing Gases. *IEEE Electron Device Letters*, **2017**, 38, 971-974 | 4.4 | 8 |
| 89 | Humidity-Sensitive Field Effect Transistor with In□□Nanoparticles as a Sensing Layer. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6656-6662 | 1.3 | 8 |
| 88 | A novel high performance junctionless FETs with saddle-gate. *Journal of Computational Electronics*, **2015**, 14, 661-668 | 1.8 | 8 |
| 87 | Negligible hysteresis of molybdenum disulfide field-effect transistors through thermal annealing. *Journal of Information Display*, **2016**, 17, 103-108 | 4.1 | 8 |
| 86 | Fundamental effects in nanoscale thermocapillary flow. *Journal of Applied Physics*, **2014**, 115, 054315 | 2.5 | 8 |
| 85 | Detection of Interleaved OFDMA Uplink Signals in the Presence of Residual Frequency Offset Using the SAGE Algorithm. *IEEE Transactions on Vehicular Technology*, **2007**, 56, 1455-1460 | 6.8 | 8 |
| 84 | Electrical and Thermal Performances of Omega-Shaped-Gate Nanowire Field Effect Transistors for Low Power Operation. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 4092-4096 | 1.3 | 8 |
| 83 | Elimination of the gate and drain bias stresses in I□V characteristics of WSe2 FETs by using dual channel pulse measurement. *Applied Physics Letters*, **2016**, 109, 053503 | 3.4 | 7 |

| | | | |
|---|---|---|---|
| 82 | Synaptic Devices Based on 3-D AND Flash Memory Architecture for Neuromorphic Computing **2019**, | | 7 |
| 81 | Unsupervised Online Learning With Multiple Postsynaptic Neurons Based on Spike-Timing-Dependent Plasticity Using a Thin-Film Transistor-Type NOR Flash Memory Array. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6050-6054 | 1.3 | 7 |
| 80 | Effects of the active layers deposition temperature on the electrical performance of p-type SnO thin-film Transistors. *Journal of the Korean Physical Society*, **2014**, 65, 286-290 | 0.6 | 7 |
| 79 | Observation of Slow Oxide Traps at MOSFETs Having Metal/High-k Gate Dielectric Stack in Accumulation Mode. *IEEE Transactions on Electron Devices*, **2010**, 57, 2697-2703 | 2.9 | 7 |
| 78 | A Highly Sensitive FET-Type Humidity Sensor with Inkjet-Printed Pt-InO Nanoparticles at Room Temperature. *Nanoscale Research Letters*, **2020**, 15, 198 | 5 | 7 |
| 77 | Impact of the Sub-Resting Membrane Potential on Accurate Inference in Spiking Neural Networks. *Scientific Reports*, **2020**, 10, 3515 | 4.9 | 6 |
| 76 | Novel Double-Gate 1T-DRAM Cell Using Nonvolatile Memory Functionality for High-Performance and Highly Scalable Embedded DRAMs. *IEEE Transactions on Electron Devices*, **2010**, 57, 614-619 | 2.9 | 6 |
| 75 | Comprehensive and accurate analysis of the working principle in ferroelectric tunnel junctions using low-frequency noise spectroscopy.. *Nanoscale*, **2022**, | 7.7 | 6 |
| 74 | A Spiking Neural Network with a Global Self-Controller for Unsupervised Learning Based on Spike-Timing-Dependent Plasticity Using Flash Memory Synaptic Devices **2019**, | | 5 |
| 73 | Characterization of a Capacitorless DRAM Cell for Cryogenic Memory Applications. *IEEE Electron Device Letters*, **2019**, 40, 1614-1617 | 4.4 | 5 |
| 72 | Analog Complementary Metal-Oxide-Semiconductor Integrate-and-Fire Neuron Circuit for Overflow Retaining in Hardware Spiking Neural Networks. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 3117-3122 | 1.3 | 5 |
| 71 | Effectiveness of a Guard Ring Utilizing an Inversion Layer Surrounding a Through Silicon Via. *IEEE Electron Device Letters*, **2015**, 36, 268-270 | 4.4 | 4 |
| 70 | GIDL Characteristics in Gated-Diode Memory String and Its Application to Current-Steering Digital-to-Analog Conversion. *IEEE Transactions on Electron Devices*, **2015**, 62, 3272-3277 | 2.9 | 4 |
| 69 | Accurate extraction of WSe2 FETs parameters by using pulsed I-V method at various temperatures. *Nano Convergence*, **2016**, 3, 31 | 9.2 | 4 |
| 68 | Pulsed I–V measurement method to obtain hysteresis-free characteristics of graphene FETs. *Semiconductor Science and Technology*, **2014**, 29, 095006 | 1.8 | 4 |
| 67 | Extraction of the Channel Mobility in InGaZnO TFTs Using Multifrequency Capacitance–Voltage Method. *IEEE Electron Device Letters*, **2012**, 33, 815-817 | 4.4 | 4 |
| 66 | High-Density Three-Dimensional Stacked nand Flash With Common Gate Structure and Shield Layer. *IEEE Transactions on Electron Devices*, **2011**, 58, 4212-4218 | 2.9 | 4 |
| 65 | Field Effect Transistor-Type Devices Using High-□ Gate Insulator Stacks for Neuromorphic Applications. *ACS Applied Electronic Materials*, **2020**, 2, 323-328 | 4 | 4 |

| | | | |
|---|---|---|---|
| 64 | Accurate identification of gas type and concentration using DNN reflecting the sensing properties of MOSFET-type gas sensor **2019**, | | 4 |
| 63 | Interlayer engineering for enhanced ferroelectric tunnel junction operations in HfO-based metal-ferroelectric-insulator-semiconductor stack. *Nanotechnology*, **2021**, 32, | 3.4 | 4 |
| 62 | Trap Profiling in Nitride Storage Layer in 3-D NAND Flash Memory Using Retention Characteristics and AC- $text{g}_{mathrm {m}}$ Method. *IEEE Electron Device Letters*, **2015**, 36, 561-563 | 4.4 | 3 |
| 61 | Vertical Inner Gate Transistors for 4F2 DRAM Cell. *IEEE Transactions on Electron Devices*, **2020**, 67, 944-948 | 2.9 | 3 |
| 60 | Novel Boosting Scheme Using Asymmetric Pass Voltage for Reducing Program Disturbance in 3-Dimensional NAND Flash Memory. *IEEE Journal of the Electron Devices Society*, **2018**, 1-1 | 2.3 | 3 |
| 59 | Layer Selection by Multi-Level Permutation in 3-D Stacked NAND Flash Memory. *IEEE Electron Device Letters*, **2016**, 37, 866-869 | 4.4 | 3 |
| 58 | Optimization of saddle junctionless FETs for extreme high integration. *Journal of Computational Electronics*, **2016**, 15, 801-808 | 1.8 | 3 |
| 57 | Analysis on New Read Disturbance Induced by Hot Carrier Injections in 3-D Channel-Stacked NAND Flash Memory. *IEEE Transactions on Electron Devices*, **2019**, 66, 3326-3330 | 2.9 | 3 |
| 56 | Flicker Noise Behavior in Resistive Memory Devices With Double-Layered Transition Metal Oxide. *IEEE Electron Device Letters*, **2013**, 34, 244-246 | 4.4 | 3 |
| 55 | Relationship Between Conduction Mechanism and Low-Frequency Noise in Polycrystalline-$hbox{TiO}_{x}$-Based Resistive-Switching Memory Devices. *IEEE Electron Device Letters*, **2012**, 33, 1063-1065 | 4.4 | 3 |
| 54 | Accurate extraction of $1/f$ noise due to random telegraph noise in gate edge current of high-k n-type metal-oxide-semiconductor field-effect transistors under accumulation mode. *Applied Physics Letters*, **2011**, 98, 023505 | 3.4 | 3 |
| 53 | Study of Si implantation into Mg-doped GaN for MOSFETs. *Physica Status Solidi C: Current Topics in Solid State Physics*, **2010**, 7, 1964-1966 | | 3 |
| 52 | Implementation of Synaptic Device Using Various High- Gate Dielectric Stacks. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 4292-4297 | 1.3 | 3 |
| 51 | Investigation on Ambipolar Current Suppression Using a Stacked Gate in an L-shaped Tunnel Field-Effect Transistor. *Micromachines*, **2019**, 10, | 3.3 | 3 |
| 50 | 3-D AND-Type Flash Memory Architecture With High-$k$ Gate Dielectric for High-Density Synaptic Devices. *IEEE Transactions on Electron Devices*, **2021**, 68, 3801-3806 | 2.9 | 3 |
| 49 | Effects of Postdeposition Annealing Ambience on NO$_2$ Gas Sensing Performance in Si-Based FET-Type Gas Sensor. *IEEE Transactions on Electron Devices*, **2022**, 1-7 | 2.9 | 3 |
| 48 | A novel high-performance H-gate U-channel junctionless FET. *Journal of Computational Electronics*, **2017**, 16, 287-295 | 1.8 | 2 |
| 47 | Analysis of Clockwise and Counter-Clockwise Hysteresis Characteristics in 3-D NAND Flash Memory Cells. *IEEE Electron Device Letters*, **2017**, 38, 867-870 | 4.4 | 2 |

| | | | |
|---|---|---|---|
| 46 | Low-Frequency Noise Characteristics in Multi-Layer WSe Field Effect Transistors with Different Contact Metals. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6422-6428 | 1.3 | 2 |
| 45 | Design Optimization and Analysis of InGaAs/InAs/InGaAs Heterojunction-Based Electron Hole Bilayer Tunneling FETs. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6070-6076 | 1.3 | 2 |
| 44 | Effect of Word-Line Bias on Linearity of Multi-Level Conductance Steps for Multi-Layer Neural Networks Based on NAND Flash Cells. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 4138-4142 | 1.3 | 2 |
| 43 | Design Consideration of Diode-Type NAND Flash Memory Cell String Having Super-Steep Switching Slope. *IEEE Journal of the Electron Devices Society*, **2016**, 4, 328-334 | 2.3 | 2 |
| 42 | Reconfigurable Cell String Having FET and Super-Steep Switching Diode Operation in 3D NAND Flash Memory **2018**, | | 2 |
| 41 | Grayscale Image Recognition Using Spike-Rate-Based Online Learning and Threshold Adjustment of Neurons in a Thin-Film Transistor-Type NOR Flash Memory Array. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6055-6060 | 1.3 | 2 |
| 40 | Switching and conduction mechanism of Cu/Si3N4/Si RRAM with CMOS compatibility **2014**, | | 2 |
| 39 | Characteristics of Elliptical Gate-All-Around SONOS Nanowire With Effective Circular Radius. *IEEE Electron Device Letters*, **2012**, 33, 1613-1615 | 4.4 | 2 |
| 38 | New Read Schemes Using Boosted Channel Potential of Adjacent Bit-Line Strings in nand Flash Memory. *IEEE Electron Device Letters*, **2012**, 33, 1198-1200 | 4.4 | 2 |
| 37 | Electrical instabilities and low-frequency noise in InGaZnO thin film transistors **2010**, | | 2 |
| 36 | Joint Common Phase Error and Channel Estimation for OFDM-based WLANs in the Presence of Wiener Phase Noise and Residual Frequency Offset **2006**, | | 2 |
| 35 | CMOS-Compatible Low-Power Gated Diode Synaptic Device for Hardware-Based Neural Network. *IEEE Transactions on Electron Devices*, **2021**, 1-6 | 2.9 | 2 |
| 34 | A Novel High Schottky Barrier Based Bilateral Gate and Assistant Gate Controlled Bidirectional Tunnel Field Effect Transistor. *IEEE Journal of the Electron Devices Society*, **2020**, 8, 976-980 | 2.3 | 2 |
| 33 | 3D AND-Type Stacked Array for Neuromorphic Systems. *Micromachines*, **2020**, 11, | 3.3 | 2 |
| 32 | Novel Program Method of String Select Transistors for Layer Selection in Channel-Stacked NAND Flash Memory. *IEEE Transactions on Electron Devices*, **2016**, 63, 3521-3526 | 2.9 | 2 |
| 31 | A novel physical unclonable function (PUF) using 16 16 pure-HfOferroelectric tunnel junction array for security applications. *Nanotechnology*, **2021**, 32, | 3.4 | 2 |
| 30 | Effect of Program Error in Memristive Neural Network With Weight Quantization. *IEEE Transactions on Electron Devices*, **2022**, 1-7 | 2.9 | 2 |
| 29 | Analysis and suppression of drain current drift in graphene FETs. *Semiconductor Science and Technology*, **2015**, 30, 105013 | 1.8 | 1 |

| | | | |
|---|---|---|---|
| 28 | Extraction of Interface Trap Density in the Region Between Adjacent Wordlines in NAND Flash Memory Strings. *IEEE Electron Device Letters*, **2015**, 36, 53-55 | 4.4 | 1 |
| 27 | Poly-silicon quantum-dot single-electron transistors. *Journal of the Korean Physical Society*, **2012**, 60, 108-112 | 0.6 | 1 |
| 26 | L-Shaped Tunneling Field-Effect Transistors for Complementary Logic Applications. *IEICE Transactions on Electronics*, **2013**, E96.C, 634-638 | 0.4 | 1 |
| 25 | Non-ideal characteristic analysis of GaN-based light-emitting diode using current-voltage (IV) and low-frequency noise experiment **2011**, | | 1 |
| 24 | Joint channel estimation and phase noise suppression for OFDM systems | | 1 |
| 23 | Channel optimized predistortion for self-heterodyne DCT-based OFDM systems. *IEEE Transactions on Consumer Electronics*, **2005**, 51, 770-775 | 4.8 | 1 |
| 22 | Branched Polyethylenimine Based Field Effect Transistor for Low Humidity Detection at Room Temperature. *IEEE Sensors Journal*, **2021**, 1-1 | 4 | 1 |
| 21 | Pruning for Hardware-Based Deep Spiking Neural Networks Using Gated Schottky Diode as Synaptic Devices. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 6603-6608 | 1.3 | 1 |
| 20 | A Systematic Compact Model Parameter Calibration with Adaptive Pattern Search Algorithm. *Applied Sciences (Switzerland)*, **2021**, 11, 4155 | 2.6 | 1 |
| 19 | A Study on the Effect of the Structural Parameters and Internal Mechanism of a Bilateral Gate-Controlled S/D Symmetric and Interchangeable Bidirectional Tunnel Field Effect Transistor. *Nanoscale Research Letters*, **2021**, 16, 102 | 5 | 1 |
| 18 | Novel Method Enabling Forward and Backward Propagations in NAND Flash Memory for On-Chip Learning. *IEEE Transactions on Electron Devices*, **2021**, 68, 3365-3370 | 2.9 | 1 |
| 17 | Review of candidate devices for neuromorphic applications **2019**, | | 1 |
| 16 | On-chip trainable hardware-based deep Q-networks approximating a backpropagation algorithm. *Neural Computing and Applications*, **2021**, 33, 9391-9402 | 4.8 | 1 |
| 15 | A source drain symmetric and interchangeable bidirectional tunneling field effect transistor. *AIP Advances*, **2018**, 8, 085318 | 1.5 | 1 |
| 14 | Core-Shell Dual-Gate Nanowire Memory as a Synaptic Device for Neuromorphic Application. *IEEE Journal of the Electron Devices Society*, **2021**, 1-1 | 2.3 | 1 |
| 13 | Highly Efficient Self-Curing Method in MOSFET Using Parasitic Bipolar Junction Transistor. *IEEE Electron Device Letters*, **2022**, 1-1 | 4.4 | 1 |
| 12 | Double-Gated Ferroelectric-Gate Field-Effect-Transistor for Processing in Memory. *IEEE Electron Device Letters*, **2021**, 1-1 | 4.4 | 0 |
| 11 | Low-Latency Spiking Neural Networks Using Pre-Charged Membrane Potential and Delayed Evaluation. *Frontiers in Neuroscience*, **2021**, 15, 629000 | 5.1 | 0 |

| | | | |
|---|---|---|---|
| 10 | Response Comparison of Resistor- and Si FET-Type Gas Sensors on the Same Substrate. *IEEE Transactions on Electron Devices*, **2021**, 68, 3552-3557 | 2.9 | 0 |
| 9 | Direct Gradient Calculation: Simple and Variation-Tolerant On-Chip Training Method for Neural Networks. *Advanced Intelligent Systems*, **2021**, 3, 2100064 | 6 | 0 |
| 8 | Effect of Lateral Charge Diffusion on Retention Characteristics of 3D NAND Flash Cells. *IEEE Electron Device Letters*, **2021**, 42, 1148-1151 | 4.4 | 0 |
| 7 | Gated Schottky Diode-Type Synaptic Device with a Field-Plate Structure to Reduce the Forward Current. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6135-6138 | 1.3 | |
| 6 | Field-Effect Transistors: Threshold Voltage Control of Multilayered MoS2 Field-Effect Transistors via Octadecyltrichlorosilane and their Applications to Active Matrixed Quantum Dot Displays Driven by Enhancement-Mode Logic Gates (Small 7/2019). *Small*, **2019**, 15, 1970037 | 11 | |
| 5 | A Simulation Study on Reducing the Grain Boundary Position Dependency in Tunneling Thin-Film Transistors Using a Wide Tunneling Area. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 6627-6631 | 1.3 | |
| 4 | Variability of DRAM Peripheral Transistor at Liquid Nitrogen Temperature. *IEEE Transactions on Electron Devices*, **2021**, 68, 1627-1632 | 2.9 | |
| 3 | Suppression of Statistical Variability in Stacked Nanosheet Using Floating Fin Structure. *IEEE Electron Device Letters*, **2021**, 1-1 | 4.4 | |
| 2 | Hardware-Based Spiking Neural Networks Using Capacitor-Less Positive Feedback Neuron Devices. *IEEE Transactions on Electron Devices*, **2021**, 68, 4766-4772 | 2.9 | |
| 1 | Novel Dual Liner Process for Side-Shielded Forksheet Device With Superior Design Margin. *IEEE Transactions on Electron Devices*, **2022**, 1-4 | 2.9 | |