In-Tak Cho

List of Publications by Year
in descending order

161	2,100	257101	315357
papers	citations	24 h-index	38 g-index

162	162	162	2232
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Water-Soluble Thin Film Transistors and Circuits Based on Amorphous Indiumâ€“Galliumâ€“Zinc Oxide. ACS Applied Materials & Interfaces, 2015, 7, 8268-8274.	4.0	113
2	FET-type gas sensors: A review. Sensors and Actuators B: Chemical, 2021, 330, 129240.	4.0	108
3	Scaling Effect on Silicon Nitride Memristor with Highly Doped Si Substrate. Small, 2018, 14, e1704062.	5.2	74
4	Silicon-Based Floating-Body Synaptic Transistor With Frequency-Dependent Short- and Long-Term Memories. IEEE Electron Device Letters, 2016, 37, 249-252.	2.2	67
5	Spiking Neural Network Using Synaptic Transistors and Neuron Circuits for Pattern Recognition With Noisy Images. IEEE Electron Device Letters, 2018, 39, 630-633.	2.2	64
6	Joint Carrier Frequency Synchronization and Channel Estimation for OFDM Systems Via the EM Algorithm. IEEE Transactions on Vehicular Technology, 2006, 55, 167-172.	3.9	60
7	Demonstration of Unsupervised Learning With Spike-Timing-Dependent Plasticity Using a TFT-Type NOR Flash Memory Array. IEEE Transactions on Electron Devices, 2018, 65, 1774-1780.	1.6	54
8	High-Density and Near-Linear Synaptic Device Based on a Reconfigurable Gated Schottky Diode. IEEE Electron Device Letters, 2017, 38, 1153-1156.	2.2	49
9	Adaptive learning rule for hardware-based deep neural networks using electronic synapse devices. Neural Computing and Applications, 2019, 31, 8101-8116.	3.2	47
10	Fluorinated CYTOP passivation effects on the electrical reliability of multilayer MoS₂ field-effect transistors. Nanotechnology, 2015, 26, 455201.	1.3	46
11	Improvement of Long-Term Durability and Bias Stress Stability in p-Type SnO Thin-Film Transistors Using a SU-8 Passivation Layer. IEEE Electron Device Letters, 2014, 35, 1260-1262.	2.2	45
12	Microwave purification of large-area horizontally aligned arrays of single-walled carbon nanotubes. Nature Communications, 2014, 5, 5332.	5.8	43
13	3-D Stacked Synapse Array Based on Charge-Trap Flash Memory for Implementation of Deep Neural Networks. IEEE Transactions on Electron Devices, 2019, 66, 420-427.	1.6	37
14	Effect of Temperature and Humidity on $hbox{NO}_{2}$ and $hbox{NH}_{3}$ Gas Sensitivity of Bottom-Gate Graphene FETs Prepared by ICP-CVD. IEEE Electron Device Letters, 2012, 33, 1084-1086.	2.2	34
15	Investigation of the charge transport mechanism and subgap density of states in p-type Cu2O thin-film transistors. Applied Physics Letters, 2013, 102, .	1.5	34
16	Neuromorphic Computing Using NAND Flash Memory Architecture With Pulse Width Modulation Scheme. Frontiers in Neuroscience, 2020, 14, 571292.	1.4	34
17	On-Chip Training Spiking Neural Networks Using Approximated Backpropagation With Analog Synaptic Devices. Frontiers in Neuroscience, 2020, 14, 423.	1.4	32
18	Threshold Voltage Fluctuation by Random Telegraph Noise in Floating Gate nand Flash Memory String. IEEE Transactions on Electron Devices, 2011, 58, 67-73.	1.6	31

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19	Low frequency noise characteristics in multilayer WSe2 field effect transistor. Applied Physics Letters, 2015, 106, .	1.5	30
20	Time and Frequency Synchronization for OFDMA Uplink System using the SAGE Algorithm. IEEE Transactions on Wireless Communications, 2007, 6, 1176-1181.	6.1	29
21	Implementation of Short-Term Plasticity and Long-Term Potentiation in a Synapse Using Si-Based Type of Charge-Trap Memory. IEEE Transactions on Electron Devices, 2015, 62, 569-573.	1.6	27
22	Ultralow power switching in a silicon-rich SiN_y/SiN_x double-layer resistive memory device. Physical Chemistry Chemical Physics, 2017, 19, 18988-18995.	1.3	27
23	Fabrication and Characterization of a Thin-Body Poly-Si 1T DRAM With Charge-Trap Effect. IEEE Electron Device Letters, 2019, 40, 566-569.	2.2	27
24	Reconfigurable Field-Effect Transistor as a Synaptic Device for XNOR Binary Neural Network. IEEE Electron Device Letters, 2019, 40, 624-627.	2.2	26
25	Effect of Temperature and Electric Field on Degradation in Amorphous InGaZnO TFTs Under Positive Gate and Drain Bias Stress. IEEE Electron Device Letters, 2014, 35, 458-460.	2.2	25
26	Single-Crystalline Si STacked ARray (STAR) NAND Flash Memory. IEEE Transactions on Electron Devices, 2011, 58, 1006-1014.	1.6	24
27	A Split-Gate Positive Feedback Device With an Integrate-and-Fire Capability for a High-Density Low-Power Neuron Circuit. Frontiers in Neuroscience, 2018, 12, 704.	1.4	24
28	1/f-Noise in AlGaN/GaN Nanowire Omega-FinFETs. IEEE Electron Device Letters, 2017, 38, 252-254.	2.2	23
29	Electrical characteristics of FinFET with vertically nonuniform source/drain doping profile. IEEE Nanotechnology Magazine, 2002, 1, 233-237.	1.1	22
30	Bias-Stress-Induced Instabilities in P-Type ${m Cu}_{2}{m O}$ Thin-Film Transistors. IEEE Electron Device Letters, 2013, 34, 647-649.	2.2	22
31	Simulation study on deep nanoscale short channel junctionless SOI FinFETs with triple-gate or double-gate structures. Journal of Computational Electronics, 2014, 13, 509-514.	1.3	22
32	Highly Selective and Low-Power Carbon Monoxide Gas Sensor Based on the Chain Reaction of Oxygen and Carbon Monoxide to WO₃. ACS Applied Materials & Interfaces, 2022, 14, 17950-17958.	4.0	22
33	Investigation of Random Telegraph Noise in Gate-Induced Drain Leakage and Gate Edge Direct Tunneling Currents of High-k MOSFETs. IEEE Transactions on Electron Devices, 2010, 57, 913-918.	1.6	21
34	A 650 V Super-Junction MOSFET With Novel Hexagonal Structure for Superior Static Performance and High BV Resilience to Charge Imbalance: A TCAD Simulation Study. IEEE Electron Device Letters, 2017, 38, 111-114.	2.2	21
35	A polycrystalline-silicon dual-gate MOSFET-based 1T-DRAM using grain boundary-induced variable resistance. Applied Physics Letters, 2019, 114, .	1.5	20
36	Comprehensive and accurate analysis of the working principle in ferroelectric tunnel junctions using low-frequency noise spectroscopy. Nanoscale, 2022, 14, 2177-2185.	2.8	20

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37	Low-Frequency Noise Properties in Double-Gate Amorphous InGaZnO Thin-Film Transistors Fabricated by Back-Channel-Etch Method. IEEE Electron Device Letters, 2015, 36, 1332-1335.	2.2	19
38	3-D Synapse Array Architecture Based on Charge-Trap Flash Memory for Neuromorphic Application. Electronics (Switzerland), 2020, 9, 57.	1.8	19
39	Effect of Program Error in Memristive Neural Network With Weight Quantization. IEEE Transactions on Electron Devices, 2022, 69, 3151-3157.	1.6	18
40	Suppression of Read Disturb Fail Caused by Boosting Hot Carrier Injection Effect for 3-D Stack NAND Flash Memories. IEEE Electron Device Letters, 2014, 35, 42-44.	2.2	17
41	Threshold Voltage Control of Multilayered MoS₂ Fieldâ€Effect Transistors via Octadecyltrichlorosilane and their Applications to Active Matrixed Quantum Dot Displays Driven by Enhancementâ€Mode Logic Gates. Small, 2019, 15, e1803852.	5.2	16
42	3-D AND-Type Flash Memory Architecture With High-Î¹ Gate Dielectric for High-Density Synaptic Devices. IEEE Transactions on Electron Devices, 2021, 68, 3801-3806.	1.6	16
43	Impact of the Sub-Resting Membrane Potential on Accurate Inference in Spiking Neural Networks. Scientific Reports, 2020, 10, 3515.	1.6	15
44	A Highly Sensitive FET-Type Humidity Sensor with Inkjet-Printed Pt-In2O3 Nanoparticles at Room Temperature. Nanoscale Research Letters, 2020, 15, 198.	3.1	15
45	Border trap characterization in amorphous indium-gallium-zinc oxide thin-film transistors with SiOX and SiNX gate dielectrics. Applied Physics Letters, 2013, 103, 142104.	1.5	14
46	Local-Degradation-Induced Threshold Voltage Shift in Turned-OFF Amorphous InGaZnO Thin Film Transistors Under AC Drain Bias Stress. IEEE Electron Device Letters, 2015, 36, 579-581.	2.2	14
47	Analysis on Program Disturbance in Channel-Stacked NAND Flash Memory With Layer Selection by Multilevel Operation. IEEE Transactions on Electron Devices, 2016, 63, 1041-1046.	1.6	14
48	Graphene electrode with tunable charge transport in thin-film transistors. Nano Research, 2018, 11, 274-286.	5.8	14
49	Electrical and Thermal Performances of Omega-Shaped-Gate Nanowire Field Effect Transistors for Low Power Operation. Journal of Nanoscience and Nanotechnology, 2020, 20, 4092-4096.	0.9	14
50	Investigation of Gate Etch Damage at Metal/High-k Gate Dielectric Stack Through Random Telegraph Noise in Gate Edge Direct Tunneling Current. IEEE Electron Device Letters, 2011, 32, 569-571.	2.2	13
51	Synaptic Devices Based on 3-D AND Flash Memory Architecture for Neuromorphic Computing. , 2019, , .		13
52	Characterization of a Capacitorless DRAM Cell for Cryogenic Memory Applications. IEEE Electron Device Letters, 2019, 40, 1614-1617.	2.2	13
53	A novel high performance junctionless FETs with saddle-gate. Journal of Computational Electronics, 2015, 14, 661-668.	1.3	12
54	Humidity-Sensitive Field Effect Transistor with In₂O₃ Nanoparticles as a Sensing Layer. Journal of Nanoscience and Nanotechnology, 2019, 19, 6656-6662.	0.9	12

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55	Novel Double-Gate 1T-DRAM Cell Using Nonvolatile Memory Functionality for High-Performance and Highly Scalable Embedded DRAMs. IEEE Transactions on Electron Devices, 2010, 57, 614-619.	1.6	11
56	Analog Complementary Metalâ€“Oxideâ€“Semiconductor Integrate-and-Fire Neuron Circuit for Overflow Retaining in Hardware Spiking Neural Networks. Journal of Nanoscience and Nanotechnology, 2020, 20, 3117-3122.	0.9	11
57	Interlayer engineering for enhanced ferroelectric tunnel junction operations in HfO _x -based metal-ferroelectric-insulator-semiconductor stack. Nanotechnology, 2021, 32, 495203.	1.3	11
58	Core-Shell Dual-Gate Nanowire Memory as a Synaptic Device for Neuromorphic Application. IEEE Journal of the Electron Devices Society, 2021, 9, 1282-1289.	1.2	11
59	Synergistic improvement of sensing performance in ferroelectric transistor gas sensors using remnant polarization. Materials Horizons, 2022, 9, 1623-1630.	6.4	11
60	Detection of Interleaved OFDMA Uplink Signals in the Presence of Residual Frequency Offset Using the SAGE Algorithm. IEEE Transactions on Vehicular Technology, 2007, 56, 1455-1460.	3.9	10
61	Negligible hysteresis of molybdenum disulfide field-effect transistors through thermal annealing. Journal of Information Display, 2016, 17, 103-108.	2.1	10
62	High-Density Reconfigurable Devices With Programmable Bottom-Gate Array. IEEE Electron Device Letters, 2017, 38, 564-567.	2.2	10
63	Pulse Biasing Scheme for the Fast Recovery of FET-Type Gas Sensors for Reducing Gases. IEEE Electron Device Letters, 2017, 38, 971-974.	2.2	10
64	Hardware-based Neural Networks using a Gated Schottky Diode as a Synapse Device. , 2018, , .		10
65	Branched Polyethylenimine-Based Field Effect Transistor for Low Humidity Detection at Room Temperature. IEEE Sensors Journal, 2022, 22, 90-98.	2.4	10
66	Elimination of the gate and drain bias stresses in Iâ€“V characteristics of WSe2 FETs by using dual channel pulse measurement. Applied Physics Letters, 2016, 109, 053503.	1.5	9
67	A Spiking Neural Network with a Global Self-Controller for Unsupervised Learning Based on Spike-Timing-Dependent Plasticity Using Flash Memory Synaptic Devices. , 2019, , .		9
68	Investigation on Ambipolar Current Suppression Using a Stacked Gate in an L-shaped Tunnel Field-Effect Transistor. Micromachines, 2019, 10, 753.	1.4	9
69	Field Effect Transistor-Type Devices Using High-Î² Gate Insulator Stacks for Neuromorphic Applications. ACS Applied Electronic Materials, 2020, 2, 323-328.	2.0	9
70	Low-Latency Spiking Neural Networks Using Pre-Charged Membrane Potential and Delayed Evaluation. Frontiers in Neuroscience, 2021, 15, 629000.	1.4	9
71	Fundamental effects in nanoscale thermocapillary flow. Journal of Applied Physics, 2014, 115, 054315.	1.1	8
72	Analysis on New Read Disturbance Induced by Hot Carrier Injections in 3-D Channel-Stacked NAND Flash Memory. IEEE Transactions on Electron Devices, 2019, 66, 3326-3330.	1.6	8

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73	Double-Gated Ferroelectric-Gate Field-Effect-Transistor for Processing in Memory. IEEE Electron Device Letters, 2021, 42, 1607-1610.	2.2	8
74	Effects of Postdeposition Annealing Ambience on NO₂ Gas Sensing Performance in Si-Based FET-Type Gas Sensor. IEEE Transactions on Electron Devices, 2022, 69, 2604-2610.	1.6	8
75	Observation of Slow Oxide Traps at MOSFETs Having Metal/High-k Gate Dielectric Stack in Accumulation Mode. IEEE Transactions on Electron Devices, 2010, 57, 2697-2703.	1.6	7
76	Effects of the active layers deposition temperature on the electrical performance of p-type SnO thin-film Transistors. Journal of the Korean Physical Society, 2014, 65, 286-290.	0.3	7
77	A novel high-performance H-gate U-channel junctionless FET. Journal of Computational Electronics, 2017, 16, 287-295.	1.3	7
78	Unsupervised Online Learning With Multiple Postsynaptic Neurons Based on Spike-Timing-Dependent Plasticity Using a Thin-Film Transistor-Type NOR Flash Memory Array. Journal of Nanoscience and Nanotechnology, 2019, 19, 6050-6054.	0.9	7
79	A Novel High Schottky Barrier Based Bilateral Gate and Assistant Gate Controlled Bidirectional Tunnel Field Effect Transistor. IEEE Journal of the Electron Devices Society, 2020, 8, 976-980.	1.2	7
80	Novel Method Enabling Forward and Backward Propagations in NAND Flash Memory for On-Chip Learning. IEEE Transactions on Electron Devices, 2021, 68, 3365-3370.	1.6	7
81	Effect of Lateral Charge Diffusion on Retention Characteristics of 3D NAND Flash Cells. IEEE Electron Device Letters, 2021, 42, 1148-1151.	2.2	7
82	Highly Efficient Self-Curing Method in MOSFET Using Parasitic Bipolar Junction Transistor. IEEE Electron Device Letters, 2022, 43, 1001-1004.	2.2	7
83	Joint Channel Estimation and Phase Noise Suppression for OFDM Systems. , 0, , .		6
84	Flicker Noise Behavior in Resistive Memory Devices With Double-Layered Transition Metal Oxide. IEEE Electron Device Letters, 2013, 34, 244-246.	2.2	6
85	Pulsedâ€“Vmeasurement method to obtain hysteresis-free characteristics of graphene FETs. Semiconductor Science and Technology, 2014, 29, 095006.	1.0	6
86	Trap Profiling in Nitride Storage Layer in 3-D NAND Flash Memory Using Retention Characteristics and AC-<inline-formula> <tex-math notation="LaTeX">$ext{g}_{mathrm {m}}$ </tex-math></inline-formula> Method. IEEE Electron Device Letters, 2015, 36, 561-563.	2.2	6
87	A novel physical unclonable function (PUF) using 16ÂÃ—Â16 pure-HfO _x ferroelectric tunnel junction array for security applications. Nanotechnology, 2021, 32, 485202.	1.3	6
88	Characteristics of Elliptical Gate-All-Around SONOS Nanowire With Effective Circular Radius. IEEE Electron Device Letters, 2012, 33, 1613-1615.	2.2	5
89	Effectiveness of a Guard Ring Utilizing an Inversion Layer Surrounding a Through Silicon Via. IEEE Electron Device Letters, 2015, 36, 268-270.	2.2	5
90	Optimization of saddle junctionless FETs for extreme high integration. Journal of Computational Electronics, 2016, 15, 801-808.	1.3	5

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91	Novel Boosting Scheme Using Asymmetric Pass Voltage for Reducing Program Disturbance in 3-Dimensional NAND Flash Memory. IEEE Journal of the Electron Devices Society, 2018, 6, 286-290.	1.2	5
92	Accurate identification of gas type and concentration using DNN reflecting the sensing properties of MOSFET-type gas sensor. , 2019, , .		5
93	Vertical Inner Gate Transistors for 4F² DRAM Cell. IEEE Transactions on Electron Devices, 2020, 67, 944-948.	1.6	5
94	Channel optimized predistortion for self-heterodyne DCT-based OFDM systems. IEEE Transactions on Consumer Electronics, 2005, 51, 770-775.	3.0	4
95	High-Density Three-Dimensional Stacked nand Flash With Common Gate Structure and Shield Layer. IEEE Transactions on Electron Devices, 2011, 58, 4212-4218.	1.6	4
96	Accurate extraction of Î”I/I due to random telegraph noise in gate edge current of high-k n-type metal-oxide-semiconductor field-effect transistors under accumulation mode. Applied Physics Letters, 2011, 98, 023505.	1.5	4
97	Relationship Between Conduction Mechanism and Low-Frequency Noise in Polycrystalline-$\hbox{TiO}_{x}$-Based Resistive-Switching Memory Devices. IEEE Electron Device Letters, 2012, 33, 1063-1065.	2.2	4
98	Extraction of the Channel Mobility in InGaZnO TFTs Using Multifrequency Capacitanceâ€“Voltage Method. IEEE Electron Device Letters, 2012, 33, 815-817.	2.2	4
99	Investigation into the effect of the variation of gate dimensions on program characteristics in 3D NAND flash array. , 2012, , .		4
100	GIDL Characteristics in Gated-Diode Memory String and Its Application to Current-Steering Digital-to-Analog Conversion. IEEE Transactions on Electron Devices, 2015, 62, 3272-3277.	1.6	4
101	Accurate extraction of WSe2 FETs parameters by using pulsed I-V method at various temperatures. Nano Convergence, 2016, 3, 31.	6.3	4
102	Layer Selection by Multi-Level Permutation in 3-D Stacked NAND Flash Memory. IEEE Electron Device Letters, 2016, 37, 866-869.	2.2	4
103	Design Optimization and Analysis of InGaAs/InAs/InGaAs Heterojunction-Based Electron Hole Bilayer Tunneling FETs. Journal of Nanoscience and Nanotechnology, 2019, 19, 6070-6076.	0.9	4
104	Effect of Word-Line Bias on Linearity of Multi-Level Conductance Steps for Multi-Layer Neural Networks Based on NAND Flash Cells. Journal of Nanoscience and Nanotechnology, 2020, 20, 4138-4142.	0.9	4
105	On-chip trainable hardware-based deep Q-networks approximating a backpropagation algorithm. Neural Computing and Applications, 2021, 33, 9391-9402.	3.2	4
106	Implementation of Synaptic Device Using Various High-k Gate Dielectric Stacks. Journal of Nanoscience and Nanotechnology, 2020, 20, 4292-4297.	0.9	4
107	Joint Common Phase Error and Channel Estimation for OFDM-based WLANs in the Presence of Wiener Phase Noise and Residual Frequency Offset. , 2006, , .		3
108	Study of Si implantation into Mgâ€doped GaN for MOSFETs. Physica Status Solidi C: Current Topics in Solid State Physics, 2010, 7, 1964-1966.	0.8	3

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109	New Read Schemes Using Boosted Channel Potential of Adjacent Bit-Line Strings in nand Flash Memory. IEEE Electron Device Letters, 2012, 33, 1198-1200.	2.2	3
110	Novel Program Method of String Select Transistors for Layer Selection in Channel-Stacked NAND Flash Memory. IEEE Transactions on Electron Devices, 2016, 63, 3521-3526.	1.6	3
111	Reconfigurable Cell String Having FET and Super-Steep Switching Diode Operation in 3D NAND Flash Memory. , 2018, , .		3
112	Review of candidate devices for neuromorphic applications. , 2019, , .		3
113	Pruning for Hardware-Based Deep Spiking Neural Networks Using Gated Schottky Diode as Synaptic Devices. Journal of Nanoscience and Nanotechnology, 2020, 20, 6603-6608.	0.9	3
114	3D AND-Type Stacked Array for Neuromorphic Systems. Micromachines, 2020, 11, 829.	1.4	3
115	A Study on the Effect of the Structural Parameters and Internal Mechanism of a Bilateral Gate-Controlled S/D Symmetric and Interchangeable Bidirectional Tunnel Field Effect Transistor. Nanoscale Research Letters, 2021, 16, 102.	3.1	3
116	Response Comparison of Resistor- and Si FET-Type Gas Sensors on the Same Substrate. IEEE Transactions on Electron Devices, 2021, 68, 3552-3557.	1.6	3
117	Direct Gradient Calculation: Simple and Variationâ€Tolerant Onâ€Chip Training Method for Neural Networks. Advanced Intelligent Systems, 2021, 3, 2100064.	3.3	3
118	CMOS-Compatible Low-Power Gated Diode Synaptic Device for Hardware- Based Neural Network. IEEE Transactions on Electron Devices, 2022, 69, 832-837.	1.6	3
119	Electrical instabilities and low-frequency noise in InGaZnO thin film transistors. , 2010, , .		2
120	L-Shaped Tunneling Field-Effect Transistors for Complementary Logic Applications. IEICE Transactions on Electronics, 2013, E96.C, 634-638.	0.3	2
121	Switching and conduction mechanism of Cu/Si3N4/Si RRAM with CMOS compatibility. , 2014, , .		2
122	1/f -noise characteristics of AlGaN/GaN omega shaped nanowire FETs. , 2016, , .		2
123	Design Consideration of Diode-Type NAND Flash Memory Cell String Having Super-Steep Switching Slope. IEEE Journal of the Electron Devices Society, 2016, 4, 328-334.	1.2	2
124	Analysis of Clockwise and Counter-Clockwise Hysteresis Characteristics in 3-D NAND Flash Memory Cells. IEEE Electron Device Letters, 2017, 38, 867-870.	2.2	2
125	A source drain symmetric and interchangeable bidirectional tunneling field effect transistor. AIP Advances, 2018, 8, 085318.	0.6	2
126	Grayscale Image Recognition Using Spike-Rate-Based Online Learning and Threshold Adjustment of Neurons in a Thin-Film Transistor-Type NOR Flash Memory Array. Journal of Nanoscience and Nanotechnology, 2019, 19, 6055-6060.	0.9	2

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127	Low-Frequency Noise Characteristics in Multi-Layer WSe₂ Field Effect Transistors with Different Contact Metals. Journal of Nanoscience and Nanotechnology, 2019, 19, 6422-6428.	0.9	2
128	A Systematic Compact Model Parameter Calibration with Adaptive Pattern Search Algorithm. Applied Sciences (Switzerland), 2021, 11, 4155.	1.3	2
129	Body-tied double-gate SONOS flash (omega flash) memory device built on bulk Si wafer. , 0, , .		1
130	Pilot symbol initiated iterative channel estimation and decoding for QAM modulated OFDM signals. , 0, , .		1
131	Extracting accurate position and energy level of oxide trap generating random telegraph noise(RTN) in recessed channel MOSFET's. , 2010, , .		1
132	Non-ideal characteristic analysis of GaN-based light-emitting diode using current-voltage (I–V) and low-frequency noise experiment. , 2011, , .		1
133	Characterization of cell to cell interference in TANOS NAND flash memory. , 2012, , .		1
134	Poly-silicon quantum-dot single-electron transistors. Journal of the Korean Physical Society, 2012, 60, 108-112.	0.3	1
135	Integrate-and-fire neuron circuit and synaptic device with a floating body MOSFET. , 2014, , .		1
136	Analysis and suppression of drain current drift in graphene FETs. Semiconductor Science and Technology, 2015, 30, 105013.	1.0	1
137	Extraction of Interface Trap Density in the Region Between Adjacent Wordlines in NAND Flash Memory Strings. IEEE Electron Device Letters, 2015, 36, 53-55.	2.2	1
138	Suppression of Statistical Variability in Stacked Nanosheet Using Floating Fin Structure. IEEE Electron Device Letters, 2021, 42, 1580-1583.	2.2	1
139	Hardware-Based Spiking Neural Networks Using Capacitor-Less Positive Feedback Neuron Devices. IEEE Transactions on Electron Devices, 2021, 68, 4766-4772.	1.6	1
140	Response Analysis of Resistor-type Gas Sensor with Bias Voltage Condition. , 2022, , .		1
141	A new CMOS pixel with lateral and vertical BJT structure. , 0, , .		0
142	A residual frequency offset compensation scheme for OFDM system via SAGE algorithm. , 0, , .		0
143	Isolation Method for Bulk FinFET without Using CMP Process. , 0, , .		0
144	Nonlinear distortion cancellation in self-heterodyne OFDM receivers over multipath fading channels. , 0, , .		0

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145	Highly scalable vertical bandgap-engineered NAND flash memory. , 2010, , .		0
146	Effect of Cu insertion layer between top electrode and switching layer on resistive switching characteristics. , 2012, , .		0
147	Investigation of conduction mechanism in Ti/Si<inf>3</inf>N<inf>4</inf>/p-Si stacked RRAM. , 2013, , .		0
148	Optimization and modeling of npn-type selector for resistive RRAM in cross-point array structure. , 2014, , .		0
149	Rapid thermal annealing effect on resistive switching in Pt/Si<inf>3</inf>N<inf>4</inf>/Ti cells. , 2014, , .		0
150	Temperature effects on current-voltage and low frequency noise characteristics of multilayer WSe<inf>2</inf> FETs. , 2015, , .		0
151	Comparison of DC, fast I-V, and pulsed I-V measurement method in multi-layer WSe<inf>2</inf> field effect transistors. , 2016, , .		0
152	Design of a high efficient fiber-to-chip coupler with reflectors. , 2016, , .		0
153	Uniformity improvement of SiNjc-based resistive switching memory by suppressed internal overshoot current. , 2017, , .		0
154	Analyzation of Positive Feedback device with Steep Subthreshold Swing Characteristics in 14 nm FinFET Technology. , 2019, , .		0
155	Gated Schottky Diode-Type Synaptic Device with a Field-Plate Structure to Reduce the Forward Current. Journal of Nanoscience and Nanotechnology, 2019, 19, 6135-6138.	0.9	0
156	Fieldâ€Effect Transistors: Threshold Voltage Control of Multilayered MoS₂ Fieldâ€Effect Transistors via Octadecyltrichlorosilane and their Applications to Active Matrixed Quantum Dot Displays Driven by Enhancementâ€Mode Logic Gates (Small 7/2019). Small, 2019, 15, 1970037.	5.2	0
157	Detection of Low Concentration NO2 gas Using Si FET-type Gas Sensor with Localized Micro-heater for Low Power Consumption. , 2019, , .		0
158	Variability of DRAM Peripheral Transistor at Liquid Nitrogen Temperature. IEEE Transactions on Electron Devices, 2021, 68, 1627-1632.	1.6	0
159	A Simulation Study on Reducing the Grain Boundary Position Dependency in Tunneling Thin-Film Transistors Using a Wide Tunneling Area. Journal of Nanoscience and Nanotechnology, 2020, 20, 6627-6631.	0.9	0
160	Novel Dual Liner Process for Side-Shielded Forksheet Device With Superior Design Margin. IEEE Transactions on Electron Devices, 2022, 69, 2232-2235.	1.6	0
161	Optimal Bias Conditions for FET-type Gas Sensors to Minimize Current Fluctuations. , 2022, , .		0