Sorin Cristoloveanu

List of Publications by Year
in descending order

158 papers	5,287 citations	117453 34 h-index	106150 65 g-index
159 all docs	159 docs citations	159 times ranked	2375 citing authors

#	Article	IF	Citations
1	Superiority of coreâ€“shell junctionless FETs. Solid-State Electronics, 2022, 194, 108313.	0.8	4
2	Band-modulation devices. , 2021, , 267-298.		0
3	Memory Operation of ZÂ²-FET Without Selector at High Temperature. IEEE Journal of the Electron Devices Society, 2021, 9, 658-662.	1.2	2
4	Electrostatic doping and related devices. , 2021, , 241-265.		0
5	Coupling effects. , 2021, , 41-70.		0
6	Diode-based characterization methods. , 2021, , 179-200.		0
7	Emerging devices. , 2021, , 299-348.		0
8	Floating-body effects. , 2021, , 115-138.		0
9	Effects of BOX thickness, silicon thickness, and backgate bias on SCE of ET-SOI MOSFETs. Microelectronic Engineering, 2021, 238, 111506.	1.1	6
10	Nanodevices Tend to Be Round. Micromachines, 2021, 12, 330.	1.4	1
11	Improved Retention Characteristics of Z2-FET Employing Half Back-Gate Control. IEEE Transactions on Electron Devices, 2021, 68, 1041-1044.	1.6	2
12	A Review on the Recent Progress of Siliconâ€onâ€Insulatorâ€Based Photodetectors. Physica Status Solidi (A) Applications and Materials Science, 2021, 218, 2000751.	0.8	16
13	Pragmatic Z2-FET compact model including DC and 1T-DRAM memory operation. Solid-State Electronics, 2021, 179, 107960.	0.8	4
14	Fabrication and characterization of GaN-based nanostructure field effect transistors. Solid-State Electronics, 2021, 184, 108079.	0.8	2
15	Intrinsic Mechanism of Mobility Collapse in Short MOSFETs. IEEE Transactions on Electron Devices, 2021, 68, 5090-5094.	1.6	7
16	Pseudo-MOSFET transient behavior: Experiments, model, substrate and temperature effect. Solid-State Electronics, 2021, 186, 108131.	0.8	0
17	Optimization of Photoelectron In-Situ Sensing Device in FD-SOI. IEEE Journal of the Electron Devices Society, 2021, 9, 187-194.	1.2	2
18	A Review of Sharp-Switching Band-Modulation Devices. Micromachines, 2021, 12, 1540.	1.4	3

#	Article	IF	Citations
19	Photodiode with low dark current built in silicon-on-insulator using electrostatic doping. Solid-State Electronics, 2020, 168, 107733.	0.8	7
20	Effect of Gate Structure on the Trapping Behavior of GaN Junctionless FinFETs. IEEE Electron Device Letters, 2020, 41, 832-835.	2.2	18
21	Persistent Floatingâ€Body Effects in Fully Depleted Siliconâ€onâ€Insulator Transistors. Physica Status Solidi (A) Applications and Materials Science, 2020, 217, 1900948.	0.8	8
22	Effects of Contact Potential and Sidewall Surface Plane on the Performance of GaN Vertical Nanowire MOSFETs for Low-Voltage Operation. IEEE Transactions on Electron Devices, 2020, 67, 1547-1552.	1.6	7
23	Deep-Depletion Effect in SOI Substrates and its Application in Photodetectors With Tunable Responsivity and Detection Range. IEEE Transactions on Electron Devices, 2020, 67, 3256-3262.	1.6	9
24	Memory Operations of Zero Impact Ionization, Zero Subthreshold Swing FET Matrix Without Selectors. IEEE Electron Device Letters, 2020, 41, 361-364.	2.2	4
25	Effects of Interface Traps and Self-Heating on the Performance of GAA GaN Vertical Nanowire MOSFET. IEEE Transactions on Electron Devices, 2020, 67, 816-821.	1.6	15
26	Novel Semiconductor devices Based on SOL Substrate. , 2020, , .		0
27	Dynamic Coupling Effect in Z²-FET and Its Application for Photodetection. IEEE Journal of the Electron Devices Society, 2019, 7, 846-854.	1.2	10
28	Esaki Diode in Undoped Silicon Film. IEEE Electron Device Letters, 2019, 40, 1346-1349.	2.2	11
29	Sharp Logic Switch Based on Band Modulation. IEEE Electron Device Letters, 2019, 40, 1852-1855.	2.2	9
30	Reliability Study of Thin-Oxide Zero-Ionization, Zero-Swing FET 1T-DRAM Memory Cell. IEEE Electron Device Letters, 2019, 40, 1084-1087.	2.2	10
31	Characteristics of band modulation FET on sub 10 nm SOI. Japanese Journal of Applied Physics, 2019, 58, SBBB07.	0.8	2
32	Carrier Lifetime Measurement in Ultrathin FD-SOI Using Virtual Diodes. IEEE Transactions on Electron Devices, 2019, 66, 1874-1880.	1.6	5
33	The concept of electrostatic doping and related devices. Solid-State Electronics, 2019, 155, 32-43.	0.8	46
34	New prospects on high on-current and steep subthreshold slope for innovative Tunnel FET architectures. Solid-State Electronics, 2019, 159, 26-37.	0.8	13
35	Impact of contact and channel resistance on the frequency-dependent capacitance and conductance of pseudo-MOSFET. Solid-State Electronics, 2019, 159, 197-203.	0.8	5
36	Deep Sub-60 mV/decade Subthreshold Swing in AlGaN/GaN FinMISHFETs with M-Plane Sidewall Channel. IEEE Transactions on Electron Devices, 2019, 66, 1699-1703.	1.6	14

#	Article	IF	Citations
37	Low-Frequency Noise Characteristics of GaN Nanowire Gate-All-Around Transistors With/Without 2-DEG Channel. IEEE Transactions on Electron Devices, 2019, 66, 1243-1248.	1.6	16
38	Temperature and Gate Leakage Influence on the Z2-FET Memory Operation. , 2019, , .		1
39	Photodiode with Low Dark Current Built in Silicon-on-Insulator by Electrostatic Doping. , 2019, , .		0
40	Trap and 1/f-noise effects at the surface and core of GaN nanowire gate-all-around FET structure. Nano Research, 2019, 12, 809-814.	5.8	14
41	Interface Coupled Photodetector (ICPD) With High Photoresponsivity Based on Silicon-on-Insulator Substrate (SOI). IEEE Journal of the Electron Devices Society, 2018, 6, 557-564.	1.2	29
42	Performance Improvement and Sub-60 mV/Decade Swing in AlGaN/GaN FinFETs by Simultaneous Activation of 2DEG and Sidewall MOS Channels. IEEE Transactions on Electron Devices, 2018, 65, 915-920.	1.6	15
43	Kink effect in ultrathin FDSOI MOSFETs. Solid-State Electronics, 2018, 143, 33-40.	0.8	9
44	Insight into carrier lifetime impact on band-modulation devices. Solid-State Electronics, 2018, 143, 41-48.	0.8	17
45	New insights on SOI Tunnel FETs with low-temperature process flow for CoolCubeâ„¢ integration. Solid-State Electronics, 2018, 144, 78-85.	0.8	8
46	Experimental Demonstration of Operational Z²-FET Memory Matrix. IEEE Electron Device Letters, 2018, 39, 660-663.	2.2	21
47	A review of the Z 2 -FET 1T-DRAM memory: Operation mechanisms and key parameters. Solid-State Electronics, 2018, 143, 10-19.	0.8	36
48	A New Photodetector on SOI. , 2018, , .		3
49	Impact of Low-Temperature Coolcubeâ„¢ Process on the Performance of FDSOI Tunnel FETs. , 2018, , .		0
50	A highly sensitive photodetector based on deepdepletion effects in SOI transistors. , 2018, , .		8
51	MSDRAM, A2RAM and Z²-FET performance benchmark for 1T-DRAM applications. , 2018, , .		8
52	Sharp switching, hysteresis-free characteristics of Z²-FET for fast logic applications. , 2018, , .		7
53	Evaluation of thin-oxide Z2-FET DRAM cell. , 2018, , .		7
54	A comprehensive model on field-effect pnpn devices (Z 2 -FET). Solid-State Electronics, 2017, 134, 1-8.	0.8	18

#	Article	IF	Citations
55	Ultrathin FDSOI four-gate transistors (G 4 -FETs). Microelectronic Engineering, 2017, 180, 1-4.	1.1	1
56	Ultra-low power 1T-DRAM in FDSOI technology. Microelectronic Engineering, 2017, 178, 245-249.	1.1	11
57	Low-Power Z2-FET Capacitorless 1T-DRAM. , 2017, , .		15
58	Evidence of Supercoupling Effect in Ultrathin Silicon Layers Using a Four-Gate MOSFET. IEEE Electron Device Letters, 2017, 38, 157-159.	2.2	24
59	Extended Analysis of the Z^{2} -FET: Operation as Capacitorless eDRAM. IEEE Transactions on Electron Devices, 2017, 64, 4486-4491.	1.6	34
60	A reconfigurable silicon-on-insulator diode with tunable electrostatic doping. Journal of Applied Physics, 2017, 122, .	1.1	16
61	First SOI Tunnel FETs with low-temperature process. , 2017, , .		1
62	Comparison for 1/ ${f}$ Noise Characteristics of AlGaN/GaN FinFET and Planar MISHFET. IEEE Transactions on Electron Devices, 2017, 64, 3634-3638.	1.6	29
63	Sharp-switching band-modulation back-gated devices in advanced FDSOI technology. Solid-State Electronics, 2017, 128, 180-186.	0.8	15
64	${Z}^{extsf {2}}$ -FET as Capacitor-Less eDRAM Cell For High-Density Integration. IEEE Transactions on Electron Devices, 2017, 64, 4904-4909.	1.6	28
65	Z2-FET SPICE model: DC and memory operation. , 2017, , .		3
66	Towards High-Voltage MOSFETs in Ultrathin FDSOI. International Journal of High Speed Electronics and Systems, 2016, 25, 1640005.	0.3	5
67	Fabrication of normally-off GaN nanowire gate-all-around FET with top-down approach. Applied Physics Letters, 2016, 109, .	1.5	23
68	Competitive 1T-DRAM in 28 nm FDSOI technology for low-power embedded memory. , 2016, , .		8
69	A sharp-switching gateless device (Z3-FET) in advanced FDSOI technology. , 2016, , .		6
70	Back-gate effects and mobility characterization in junctionless transistor. Solid-State Electronics, 2016, 125, 154-160.	0.8	7
71	A band-modulation device in advanced FDSOI technology: Sharp switching characteristics. Solid-State Electronics, 2016, 125, 103-110.	0.8	8
72	Novel FDSOI band-modulation device: Z2-FET with Dual Ground Planes. , 2016, , .		7

#	Article	IF	Citations
73	A Review of Sharp-Switching Devices for Ultra-Low Power Applications. IEEE Journal of the Electron Devices Society, 2016, 4, 215-226.	1.2	113
74	Fabrication and electrical characterizations of SGOI tunnel FETs with gate length down to 50 nm. Solid-State Electronics, 2016, 115, 167-172.	0.8	16
75	Electrical Characterization of FDSOI by Capacitance Measurements in Gated p-i-n Diodes. IEEE Transactions on Electron Devices, 2016, 63, 982-989.	1.6	8
76	A sharp-switching device with free surface and buried gates based on band modulation and feedback mechanisms. Solid-State Electronics, 2016, 116, 8-11.	0.8	20
77	Properties and mechanisms of Z2-FET at variable temperature. Solid-State Electronics, 2016, 115, 201-206.	0.8	21
78	CMOS-compatible FDSOI bipolar-enhanced tunneling FET. , 2015, , .		6
79	Sharp-switching Z²-FET device in 14 nm FDSOI technology. , 2015, , .		14
80	Fabrication of high performance AlGaN/GaN FinFET by utilizing anisotropic wet etching in TMAH solution. , 2015, , .		3
81	Demonstration of Unified Memory in FinFETs. , 2015, , .		0
82	Experimental investigations of SiGe channels for enhancing the SGOI tunnel FETs performance. , 2015, , .		9
83	Effects of sidewall MOS channel on performance of AlGaN/GaN FinFET. Microelectronic Engineering, 2015, 147, 155-158.	1.1	19
84	Unusual gate coupling effect in extremely thin and short FDSOI MOSFETs. Microelectronic Engineering, 2015, 147, 159-164.	1.1	6
85	Parasitic bipolar effect in ultra-thin FD SOI MOSFETs. Solid-State Electronics, 2015, 112, 29-36.	0.8	10
86	Supercoupling effect in short-channel ultrathin fully depleted silicon-on-insulator transistors. Journal of Applied Physics, 2015, 118, .	1.1	26
87	Demonstration of Unified Memory in FinFETs. International Journal of High Speed Electronics and Systems, 2014, 23, 1450019.	0.3	1
88	Room to High Temperature Measurements of Flexible SOI FinFETs With Sub-20-nm Fins. IEEE Transactions on Electron Devices, 2014, 61, 3978-3984.	1.6	21
89	Mobility Investigation by Geometrical Magnetoresistance in Fully Depleted MOSFETs and FinFETs. IEEE Transactions on Electron Devices, 2014, 61, 1979-1986.	1.6	17
90	Characteristics of GaN and AlGaN/GaN FinFETs. Solid-State Electronics, 2014, 97, 66-75.	0.8	35

#	Article	IF	Citations
91	Electron-Hole Bilayer TFET: Experiments and Comments. IEEE Transactions on Electron Devices, 2014, 61, 2674-2681.	1.6	40
92	Overestimation of Short-Channel Effects Due to Intergate Coupling in Advanced FD-SOI MOSFETs. IEEE Transactions on Electron Devices, 2014, 61, 3274-3281.	1.6	10
93	Z2-FET: A promising FDSOI device for ESD protection. Solid-State Electronics, 2014, 97, 23-29.	0.8	37
94	High-Performance GaN-Based Nanochannel FinFETs With/Without AlGaN/GaN Heterostructure. IEEE Transactions on Electron Devices, 2013, 60, 3012-3018.	1.6	98
95	Bias-Engineered Mobility in Advanced FD-SOI MOSFETs. IEEE Electron Device Letters, 2013, 34, 840-842.	2.2	14
96	Experimental Investigation of the Tunneling Injection Boosters for Enhanced I_{ON} ETSOI Tunnel FET. IEEE Transactions on Electron Devices, 2013, 60, 4079-4084.	1.6	22
97	Performance improvement of normally off AlGaN/GaN FinFETs with fully gate-covered nanochannel. Solid-State Electronics, 2013, 89, 124-127.	0.8	9
98	Progress in Z2-FET 1T-DRAM: Retention time, writing modes, selective array operation, and dual bit storage. Solid-State Electronics, 2013, 84, 147-154.	0.8	60
99	A systematic study of the sharp-switching Z2-FET device: From mechanism to modeling and compact memory applications. Solid-State Electronics, 2013, 90, 2-11.	0.8	56
100	Characterization of heavily doped SOI wafers under pseudo-MOSFET configuration. Solid-State Electronics, 2013, 90, 65-72.	0.8	20
101	Heterojunction-Free GaN Nanochannel FinFETs With High Performance. IEEE Electron Device Letters, 2013, 34, 381-383.	2.2	48
102	Novel Bipolar-Enhanced Tunneling FET With Simulated High On-Current. IEEE Electron Device Letters, 2013, 34, 24-26.	2.2	23
103	Notice of Removal: Fabrication and validation of A2RAM memory cells on SOI and bulk substrates - Withdrawn. , 2013, , .		1
104	Innovative ESD protections for UTBB FD-SOI technology. , 2013, , .		29
105	Adaptation of the pseudo-metalâ€“oxideâ€“semiconductor field effect transistor technique to ultrathin siliconâ€“on-insulator wafers characterization: Improved set-up, measurement procedure, parameter extraction, and modeling. Journal of Applied Physics, 2013, 114, 164502.	1.1	15
106	Experimental Demonstration of Capacitorless A2RAM Cells on Silicon-on-Insulator. IEEE Electron Device Letters, 2012, 33, 1717-1719.	2.2	48
107	A Compact Capacitor-Less High-Speed DRAM Using Field Effect-Controlled Charge Regeneration. IEEE Electron Device Letters, 2012, 33, 179-181.	2.2	103
108	A feedback silicon-on-insulator steep switching device with gate-controlled carrier injection. Solid-State Electronics, 2012, 76, 109-111.	0.8	65

#	Article	IF	Citations
109	FDSOI devices: A solution to achieve low junction leakage with low temperature processes (≤ 650°C). , 2012, , .		6
110	Electrical properties of P-MOSFETs on amorphized and regrown (110) SOI film for hybrid orientation technology. Journal of the Korean Physical Society, 2012, 60, 1713-1716.	0.3	0
111	Mobility Enhancement by Back-Gate Biasing in Ultrathin SOI MOSFETs With Thin BOX. IEEE Electron Device Letters, 2012, 33, 348-350.	2.2	37
112	Tunneling FETs on SOI: Suppression of ambipolar leakage, low-frequency noise behavior, and modeling. Solid-State Electronics, 2011, 65-66, 226-233.	0.8	103
113	Novel Capacitorless 1T-DRAM Cell for 22-nm Node Compatible With Bulk and SOI Substrates. IEEE Transactions on Electron Devices, 2011, 58, 2371-2377.	1.6	46
114	Double-gate 1T-DRAM cell using nonvolatile memory function for improved performance. Solid-State Electronics, 2011, 59, 39-43.	0.8	5
115	Why the Universal Mobility Is Not. IEEE Transactions on Electron Devices, 2010, 57, 1327-1333.	1.6	33
116	Dynamic body potential variation in FD SOI MOSFETs operated in deep non-equilibrium regime: Model and applications. Solid-State Electronics, 2010, 54, 104-114.	0.8	22
117	SOI promises for speed, energy and memory. , 2010, , .		0
118	Advances in the pseudo-MOSFET characterization method. , 2010, , .		1
119	A-RAM Memory Cell: Concept and Operation. IEEE Electron Device Letters, 2010, 31, 972-974.	2.2	42
120	In Situ Comparison of Si/High- $kappa$ and $hbox{Si}/ hbox{SiO}_{2}$ Channel Properties in SOI MOSFETs. IEEE Electron Device Letters, 2009, 30, 1075-1077.	2.2	25
121	Dimensional effects and scalability of Meta-Stable Dip (MSD) memory effect for 1T-DRAM SOI MOSFETs. Solid-State Electronics, 2009, 53, 1280-1286.	0.8	17
122	Micro and nano on insulator. Physica Status Solidi C: Current Topics in Solid State Physics, 2008, 5, 3588-3593.	0.8	1
123	Threshold voltage in ultra thin FDSOI CMOS : Advanced triple interface model and experimental devices. , 2008, , .		11
124	High-$kappa$ and Metal-Gate pMOSFETs on GeOI Obtained by Ge Enrichment: Analysis of ON and OFF Performances. IEEE Electron Device Letters, 2008, 29, 635-637.	2.2	20
125	A Capacitorless 1T-DRAM on SOI Based on Dynamic Coupling and Double-Gate Operation. IEEE Electron Device Letters, 2008, 29, 795-798.	2.2	87
126	Thin film fully-depleted SOI four-gate transistors. Solid-State Electronics, 2007, 51, 278-284.	0.8	22

#	Article	IF	Citations
127	Innovating SOI memory devices based on floating-body effects. Solid-State Electronics, 2007, 51, 1252-1262.	0.8	40
128	Depletion-All-Around Operation of the SOI Four-Gate Transistor. IEEE Transactions on Electron Devices, 2007, 54, 323-331.	1.6	40
129	A Model of Fringing Fields in Short-Channel Planar and Triple-Gate SOI MOSFETs. IEEE Transactions on Electron Devices, 2007, 54, 1366-1375.	1.6	56
130	Ultra-thin fully-depleted SOI MOSFETs: Special charge properties and coupling effects. Solid-State Electronics, 2007, 51, 239-244.	0.8	121
131	Low-frequency noise in SOI four-gate transistors. IEEE Transactions on Electron Devices, 2006, 53, 829-835.	1.6	48
132	Analytical modeling of the two-dimensional potential distribution and threshold voltage of the SOI four-gate transistor. IEEE Transactions on Electron Devices, 2006, 53, 2569-2577.	1.6	49
133	A new memory effect (MSD) in fully depleted SOI MOSFETs. Solid-State Electronics, 2005, 49, 1547-1555.	0.8	50
134	Coupling effect between the front and back interfaces in thin SOI MOSFETs. Microelectronic Engineering, 2005, 80, 245-248.	1.1	20
135	Transition from partial to full depletion in silicon-on-insulator transistors: Impact of channel length. Applied Physics Letters, 2004, 84, 1192-1194.	1.5	21
136	Investigation of the Four-Gate Action in<tex>$hbox G^4$</tex>-FETs. IEEE Transactions on Electron Devices, 2004, 51, 1931-1935.	1.6	53
137	Determination of film and surface recombination in thin-film SOI devices using gated-diode technique. Solid-State Electronics, 2004, 48, 389-399.	0.8	23
138	Gate-induced floating-body effect in fully-depleted SOI MOSFETs with tunneling oxide and back-gate biasing. Solid-State Electronics, 2004, 48, 1243-1247.	0.8	46
139	Ultimately thin double-gate SOI MOSFETs. IEEE Transactions on Electron Devices, 2003, 50, 830-838.	1.6	253
140	Frontiers of silicon-on-insulator. Journal of Applied Physics, 2003, 93, 4955-4978.	1.1	599
141	FARâ€“FUTURE TRENDS IN SOI TECHNOLOGY: A GUESS. , 2003, , .		0
142	THE MULTIPLE-GATE MOS-JFET TRANSISTOR. International Journal of High Speed Electronics and Systems, 2002, 12, 511-520.	0.3	52
143	Fringing fields in sub-0.1 Î¼m fully depleted SOI MOSFETs: optimization of the device architecture. Solid-State Electronics, 2002, 46, 373-378.	0.8	146
144	Double-Gate MOSFETs: Is Gate Alignment Mandatory?. , 2001, , .		15

#	Article	IF	Citations
145	A review of the pseudo-MOS transistor in SOI wafers: operation, parameter extraction, and applications. IEEE Transactions on Electron Devices, 2000, 47, 1018-1027.	1.6	185
146	Recombination current modeling and carrier lifetime extraction in dual-gate fully-depleted SOI devices. IEEE Transactions on Electron Devices, 1999, 46, 1503-1509.	1.6	26
147	Carrier lifetime extraction in fully depleted dual-gate SOI devices. IEEE Electron Device Letters, 1999, 20, 209-211.	2.2	8
148	Introduction to Silicon On Insulator materials and devices. Microelectronic Engineering, 1997, 39, 145-154.	1.1	20
149	Model for carrier lifetime extraction from pseudo-MOSFET transients. Electronics Letters, 1996, 32, 2021.	0.5	17
150	Electrical Characterization of Silicon-on-Insulator Materials and Devices. , 1995, , .		327
151	Subthreshold kinks in fully depleted SOI MOSFET's. IEEE Electron Device Letters, 1995, 16, 542-544.	2.2	28
152	Investigation of floating body effects in siliconâ€onâ€insulator metalâ€oxideâ€semiconductor fieldâ€effect transistors. Journal of Applied Physics, 1991, 70, 3912-3919.	1.1	28
153	Interface coupling effects in thin silicon-on-insulator MOSFET's. Superlattices and Microstructures, 1990, 8, 111-116.	1.4	13
154	Characterization of carrier generation in enhancement-mode SOI MOSFET's. IEEE Electron Device Letters, 1990, 11, 409-411.	2.2	77
155	Double-gate silicon-on-insulator transistor with volume inversion: A new device with greatly enhanced performance. IEEE Electron Device Letters, 1987, 8, 410-412.	2.2	643
156	Silicon films on sapphire. Reports on Progress in Physics, 1987, 50, 327-371.	8.1	53
157	Mobility issues in ultra-thin SOI MOSFETs: thickness variations, GIFBE and coupling effects. , 0, , .		3
158	Depletion-all-around in SOI G/sup 4/-FETs: a conduction mechanism with high performance. , 0, , .		3