# Maurits Ortmanns

List of Publications by Year
in descending order

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| 88 | 1,437 | 567281 | 395702 |
|---|---|---|---|
| papers | citations | 15 h-index | 33 g-index |

| 88 | 88 | 88 | 881 |
|---|---|---|---|
| all docs | docs citations | times ranked | citing authors |

| # | Article | IF | Citations |
|---|---|---|---|
| 1 | A 0.9-V DAC-Calibration-Free Continuous-Time Incremental Deltaâ€“Sigma Modulator Achieving 97-dB SFDR at 2 MS/s in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2022, 57, 3407-3417. | 5.4 | 10 |
| 2 | Wideband Continuous-Time MASH Delta-Sigma Modulators: A Tutorial Review. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2623-2628. | 3.0 | 7 |
| 3 | A Direct Digitizing Chopped Neural Recorder Using a Body-Induced Offset Based DC Servo Loop. IEEE Transactions on Biomedical Circuits and Systems, 2022, 16, 409-418. | 4.0 | 8 |
| 4 | An Integrator-Differentiator Transimpedance Amplifier Using Tunable Linearized High-Value Multi-Element Pseudo-Resistors. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 3150-3163. | 5.4 | 1 |
| 5 | Comparison Study of DAC Realizations in Current Input CTÎ£Î” Modulators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 111-115. | 3.0 | 0 |
| 6 | Input Referred Noise of VCO-Based Comparators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 82-86. | 3.0 | 3 |
| 7 | Noise Analysis of Charge-Balanced Readout Circuits for MEMS Accelerometers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 175-184. | 5.4 | 4 |
| 8 | Using Polynomial Interpolation for Reproducing Multi-Valued Responses of Physical Unclonable Functions on FPGAs. , 2021, , . | | 4 |
| 9 | A PCB-Based 24-Ch. MEA-EIS Allowing Fast Measurement of TEER. IEEE Sensors Journal, 2021, 21, 13048-13059. | 4.7 | 4 |
| 10 | A Chopped Neural Front-End Featuring Input Impedance Boosting With Suppressed Offset-Induced Charge Transfer. IEEE Transactions on Biomedical Circuits and Systems, 2021, 15, 402-411. | 4.0 | 14 |
| 11 | A High-Voltage Compliance, 32-Channel Digitally Interfaced Neuromodulation System on Chip. IEEE Journal of Solid-State Circuits, 2021, 56, 2476-2487. | 5.4 | 23 |
| 12 | Erratum to â€œA High-Voltage Compliance, 32-Channel Digitally Interfaced Neuromodulation System-on-Chipâ€• IEEE Journal of Solid-State Circuits, 2021, 56, 3203-3203. | 5.4 | 0 |
| 13 | A Multilevel Coding Scheme for Multi-Valued Physical Unclonable Functions. IEEE Transactions on Information Forensics and Security, 2021, 16, 3814-3827. | 6.9 | 5 |
| 14 | Low-Noise Readout Circuit for an Automotive MEMS Accelerometer. IEEE Open Journal of the Solid-State Circuits Society, 2021, 1, 140-148. | 2.7 | 7 |
| 15 | Nonlinearity Modeling for Mixed-Signal Inference Accelerators in Training Frameworks. , 2021, , . | | 0 |
| 16 | A 76.6-dB-SNDR 50-MHz-BW 29.2-mW Multi-Bit CT Sturdy MASH With DAC Non-Linearity Tolerance. IEEE Journal of Solid-State Circuits, 2020, 55, 344-355. | 5.4 | 38 |
| 17 | FIR DACs in CT Incremental Delta-Sigma Modulators. , 2020, , . | | 3 |
| 18 | A 14b, Twofold Time-Interleaved Incremental Î”Î£ ADC Using Hardware Sharing. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3681-3692. | 5.4 | 8 |

| # | Article | IF | Citations |
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| 19 | Performance Evaluation of Incremental Sigma-Delta ADCs Based on their NTF. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2813-2817. | 3.0 | 3 |
| 20 | Normalization and Multi-Valued Symbol Extraction From RO-PUFs for Enhanced Uniform Probability Distributions. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3372-3376. | 3.0 | 12 |
| 21 | Design Approach for Ring Amplifiers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3444-3457. | 5.4 | 2 |
| 22 | Efficient High-Resolution Nyquist ADCs. , 2020, , 41-57. | | 2 |
| 23 | An Automated Design Environment for CT Incremental Sigma-Delta ADCs. , 2020, , . | | 0 |
| 24 | A Continuous-Time Delta-Sigma Modulator Using a Modified Instrumentation Amplifier and Current Reuse DAC for Neural Recording. IEEE Journal of Solid-State Circuits, 2019, 54, 2879-2891. | 5.4 | 28 |
| 25 | A 94.3-dB SFDR, 91.5-dB DR, and 200-kS/s CT Incremental Deltaâ€“Sigma Modulator With Differentially Reset FIR Feedback. IEEE Solid-State Circuits Letters, 2019, 2, 87-90. | 2.0 | 20 |
| 26 | Comparison of Direct Digitization Current Sensing Circuits for EIS. , 2019, , . | | 1 |
| 27 | A Dynamic Power Reduction Technique for Incremental $DeltaSigma$ Modulators. IEEE Journal of Solid-State Circuits, 2019, 54, 1455-1467. | 5.4 | 29 |
| 28 | In-depth Analysis and Enhancements of RO-PUFs with a Partial Reconfiguration Framework on Xilinx Zynq-7000 SoC FPGAs. , 2019, , . | | 17 |
| 29 | An Evaluation Study of Various Excitation Signals for Electrical Impedance Spectroscopy. , 2019, , . | | 9 |
| 30 | Input Referred Comparator Noise in SAR ADCs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 718-722. | 3.0 | 7 |
| 31 | Comparison of Different Precision Pseudo Resistor Realizations in the DC-Feedback of Capacitive Transimpedance Amplifiers. , 2019, , . | | 1 |
| 32 | A 24-Ch. Multi-Electrode Array Allowing Fast EIS to Determine Transepithelial Electrical Resistance. , 2019, , . | | 2 |
| 33 | A 94.3-dB SFDR, 91.5-dB DR, and 200-kS/s CT Incremental Deltaâ€“Sigma Modulator With Differentially Reset FIR Feedback. , 2019, , . | | 3 |
| 34 | On the Signal Filtering Property of CT Incremental Sigmaâ€“Delta ADCs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1780-1784. | 3.0 | 20 |
| 35 | Towards Low-Cost, High-Sensitivity Point-of-Care Diagnostics Using VCO-Based ESR-on-a-Chip Detectors. IEEE Sensors Journal, 2019, 19, 8995-9003. | 4.7 | 13 |
| 36 | A Nyquist Rate SAR ADC Employing Incremental Sigma Delta DAC Achieving Peak SFDR = 107 dB at 80 kS/s. IEEE Journal of Solid-State Circuits, 2018, 53, 1493-1507. | 5.4 | 14 |

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| 37 | A 0.1% THD, 1-M<inline-formula> <tex-math notation="LaTeX">$Omega$ </tex-math> </inline-formula> to 1-G<inline-formula> <tex-math notation="LaTeX">$Omega$ </tex-math> </inline-formula> Tunable, Temperature-Compensated Transimpedance Amplifier Using a Multi-Element Pseudo-Resistor. IEEE Journal of Solid-State Circuits, 2018, 53, 1913-1923. | 5.4 | 54 |
| 38 | A Neuromodulator Frontend With Reconfigurable Class-B Current and Voltage Controlled Stimulator. IEEE Solid-State Circuits Letters, 2018, 1, 54-57. | 2.0 | 17 |
| 39 | Improved SQNR and MSA in Incremental <inline-formula> <tex-math notation="LaTeX">$Delta Sigma$ </tex-math> </inline-formula> Modulators by Using a Recuperation Phase. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 557-561. | 3.0 | 9 |
| 40 | Efficient implementation and stability analysis of a HV-CMOS current/voltage mode stimulator. , 2018, , . | | 4 |
| 41 | A Low Distortion Continuous Time Sigma Delta Modulator using a High Input Impedance Instrumentation Amplifier for Neural Recording. , 2018, , . | | 2 |
| 42 | On the Optimization of DT Incremental Sigma-Delta Modulators in Combination with CoI Reconstruction Filters. , 2018, , . | | 3 |
| 43 | A 0.4-V <inline-formula> <tex-math notation="LaTeX">$G_{m}$ </tex-math> </inline-formula>â€“<inline-formula> <tex-math notation="LaTeX">$C$ </tex-math> </inline-formula> Proportional-Integrator-Based Continuous-Time <inline-formula> <tex-math notation="LaTeX">$DeltaSigma$ </tex-math> </inline-formula> Modulator With 50. IEEE Journal of Solid-State Circuits, 2018, 53, 3256-3267. | 5.4 | 9 |
| 44 | An Integrator-Differentiator TIA Using a Multi-Element Pseudo-Resistor in its DC Servo Loop for Enhanced Noise Performance. , 2018, , . | | 9 |
| 45 | Comparison Study of Integrated Potentiostats: Resistive-TIA, Capacitive-TIA, CT Î£Î” Modulator. , 2018, , . | | 20 |
| 46 | VCO-based ESR-on-a-chip as a tool for low-cost, high-sensitivity food quality control. , 2017, , . | | 8 |
| 47 | Evaluation of single-bit sigma-delta modulator DAC for electrical impedance spectroscopy. , 2017, , . | | 7 |
| 48 | VCO-based ESR-on-a-chip as a tool for low-cost, high-sensitivity point-of-care diagnostics. , 2017, , . | | 2 |
| 49 | Integrated Circuit Technology for Next Generation Point-of-Care Spectroscopy Applications. , 2017, 55, 143-151. | | 9 |
| 50 | A bidirectional neural interface featuring a tunable recorder and electrode impedance estimation. , 2016, , . | | 9 |
| 51 | A bidirectional neural interface IC with high voltage compliance and spectral separation. , 2016, , . | | 8 |
| 52 | An array of fully-integrated quadrature TX/RX NMR field probes for MRI trajectory mapping. , 2016, , . | | 22 |
| 53 | A 10 MHz Bandwidth, 70 dB SNDR Continuous Time Delta-Sigma Modulator With Digitally Improved Reconfigurable Blocker Rejection. IEEE Journal of Solid-State Circuits, 2016, 51, 660-670. | 5.4 | 25 |
| 54 | A 72 dB DR, CT Î”Î£ Modulator Using Digitally Estimated, Auxiliary DAC Linearization Achieving 88 fJ/conv-step in a 25 MHz BW. IEEE Journal of Solid-State Circuits, 2014, 49, 392-404. | 5.4 | 55 |

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| 55 | A GPU-Accelerated Web-Based Synthesis Tool for CT Sigma-Delta Modulators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 1429-1441. | 5.4 | 44 |
| 56 | Calculating transfer functions of CT sigma-delta modulators with arbitrary DAC waveforms. , 2013, , . | | 9 |
| 57 | Frequency noise of CMOS LC tank oscillators operating in weak inversion. , 2013, , . | | 4 |
| 58 | Active Integrated Tracking Detectors for MRI-Guided Interventions. Biomedizinische Technik, 2012, 57, . | 0.8 | 0 |
| 59 | A Neural Stimulator Frontend With High-Voltage Compliance and Programmable Pulse Shape for Epiretinal Implants. IEEE Journal of Solid-State Circuits, 2012, 47, 244-256. | 5.4 | 179 |
| 60 | An 8.5 mW Continuous-Time $Delta Sigma $ Modulator With 25 MHz Bandwidth Using Digital Background DAC Linearization to Achieve 63.5 dB SNDR and 81 dB SFDR. IEEE Journal of Solid-State Circuits, 2011, 46, 2869-2881. | 5.4 | 79 |
| 61 | Experimental results on power efficient single-poly floating gate rectifiers. , 2009, , . | | 11 |
| 62 | Systematic approach to the synthesis of continuous-time cascaded sigmaâ€“delta modulators. Analog Integrated Circuits and Signal Processing, 2009, 60, 155-164. | 1.4 | 4 |
| 63 | High efficiency, low-voltage and self-adjusting charge pump with enhanced impedance matching. , 2008, , . | | 7 |
| 64 | A low-power differential common-gate LNA. , 2008, , . | | 9 |
| 65 | Design of current reuse CMOS LC-VCO. , 2008, , . | | 4 |
| 66 | A 0:5V rail-to-rail 1.5 μW CMOS amplifier for micro-energy harvesting applications. , 2008, , . | | 5 |
| 67 | A dynamic-Element-Matching architecture using individual element error shaping. , 2008, , . | | 0 |
| 68 | Reliability study of single-poly floating gates in 0.13 μm CMOS for use in field programmable analog arrays. , 2008, , . | | 0 |
| 69 | High-bandwidth floating gate CMOS rectifiers with reduced voltage drop. , 2008, , . | | 13 |
| 70 | Optimized scheme for power-of-two coefficient approximation for low power decimation filters in sigma delta ADCs. , 2008, , . | | 4 |
| 71 | A hexagonal Field Programmable Analog Array consisting of 55 digitally tunable OTAs. , 2008, , . | | 5 |
| 72 | Fully CMOS integrated active rectifier without voltage drop. , 2008, , . | | 12 |

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| 73 | Analysis of digital gain error compensation in continuous-time cascaded sigma-delta modulators. , 2008, , . | | 1 |
| 74 | A Switchable Folded-Cascode OTA without Transmission Gates in the Signal Path. , 2008, , . | | 3 |
| 75 | An Unscented Kalman Filter for the estimation of circuit nonidealities with implicit decimation in continuous-time multibit Sigma-Delta modulators. Midwest Symposium on Circuits and Systems, 2007, , . | 1.0 | 4 |
| 76 | Systematic approach to the synthesis of continuous-time cascaded Sigma-Delta modulators. Midwest Symposium on Circuits and Systems, 2007, , . | 1.0 | 3 |
| 77 | Estimating Circuit Nonidealities of Continuous-Time Multibit Delta-Sigma Modulators. , 2007, , . | | 4 |
| 78 | On the Implicit Anti-Aliasing Feature of Continuous-Time Multistage Noise-Shaping Sigma-Delta Modulators. , 2007, , . | | 1 |
| 79 | A Method for the Discrete-Time Simulation of Continuous-Time Sigma-Delta Modulators. , 2007, , . | | 24 |
| 80 | A 232-Channel Epiretinal Stimulator ASIC. IEEE Journal of Solid-State Circuits, 2007, 42, 2946-2959. | 5.4 | 204 |
| 81 | CMOS Integrated Highly Efficient Full Wave Rectifier. , 2007, , . | | 61 |
| 82 | Charge Balancing in Functional Electrical Stimulators: A Comparative Study. , 2007, , . | | 29 |
| 83 | A comparative study of CMOS LNAs. , 2007, , . | | 7 |
| 84 | A Study on self-timed asynchronous subthreshold logic. , 2007, , . | | 10 |
| 85 | DISCO - A toolbox for the discrete-time simulation of continuous-time Sigma-Delta modulators using MATLAB™. Midwest Symposium on Circuits and Systems, 2007, , . | 1.0 | 10 |
| 86 | Time-Continuous Delta-Sigma A/D Converters: From Theory to Practical Implementation. , 2006, , . | | 3 |
| 87 | Implementation and Analysis of Power Consumption for a Power Optimized Decimator Designed for Cascaded Sigma-Delta A/D Converters. Midwest Symposium on Circuits and Systems, 2006, , . | 1.0 | 4 |
| 88 | Compensation of Finite Gain-Bandwidth Induced Errors in Continuous-Time Sigmaâ€“Delta Modulators. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2004, 51, 1088-1099. | 0.1 | 86 |