

Maurits Ortmanns

List of Publications by Year in descending order

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88
papers

1,437
citations

567281

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395702

33
g-index

88
all docs

88
docs citations

88
times ranked

881
citing authors

#	ARTICLE	IF	CITATIONS
1	A 232-Channel Epiretinal Stimulator ASIC. IEEE Journal of Solid-State Circuits, 2007, 42, 2946-2959.	5.4	204
2	A Neural Stimulator Frontend With High-Voltage Compliance and Programmable Pulse Shape for Epiretinal Implants. IEEE Journal of Solid-State Circuits, 2012, 47, 244-256.	5.4	179
3	Compensation of Finite Gain-Bandwidth Induced Errors in Continuous-Time Sigma-Delta Modulators. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2004, 51, 1088-1099.	0.1	86
4	An 8.5 mW Continuous-Time $\Delta\Sigma$ Modulator With 25 MHz Bandwidth Using Digital Background DAC Linearization to Achieve 63.5 dB SNDR and 81 dB SFDR. IEEE Journal of Solid-State Circuits, 2011, 46, 2869-2881.	5.4	79
5	CMOS Integrated Highly Efficient Full Wave Rectifier. , 2007, , .		61
6	A 72 dB DR, CT $\Delta\Sigma$ Modulator Using Digitally Estimated, Auxiliary DAC Linearization Achieving 88 f/conv-step in a 25 MHz BW. IEEE Journal of Solid-State Circuits, 2014, 49, 392-404.	5.4	55
7	A 0.1% THD, 1-MHz $\Delta\Sigma$ Modulator Using Digitally Estimated, Auxiliary DAC Linearization Achieving 88 f/conv-step in a 25 MHz BW. IEEE Journal of Solid-State Circuits, 2018, 53, 1913-1923.	5.4	54
8	A GPU-Accelerated Web-Based Synthesis Tool for CT Sigma-Delta Modulators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 1429-1441.	5.4	44
9	A 76.6-dB-SNDR 50-MHz-BW 29.2-mW Multi-Bit CT Sturdy MASH With DAC Non-Linearity Tolerance. IEEE Journal of Solid-State Circuits, 2020, 55, 344-355.	5.4	38
10	Charge Balancing in Functional Electrical Stimulators: A Comparative Study. , 2007, , .		29
11	A Dynamic Power Reduction Technique for Incremental $\Delta\Sigma$ Modulators. IEEE Journal of Solid-State Circuits, 2019, 54, 1455-1467.	5.4	29
12	A Continuous-Time Delta-Sigma Modulator Using a Modified Instrumentation Amplifier and Current Reuse DAC for Neural Recording. IEEE Journal of Solid-State Circuits, 2019, 54, 2879-2891.	5.4	28
13	A 10 MHz Bandwidth, 70 dB SNDR Continuous Time Delta-Sigma Modulator With Digitally Improved Reconfigurable Blocker Rejection. IEEE Journal of Solid-State Circuits, 2016, 51, 660-670.	5.4	25
14	A Method for the Discrete-Time Simulation of Continuous-Time Sigma-Delta Modulators. , 2007, , .		24
15	A High-Voltage Compliance, 32-Channel Digitally Interfaced Neuromodulation System on Chip. IEEE Journal of Solid-State Circuits, 2021, 56, 2476-2487.	5.4	23
16	An array of fully-integrated quadrature TX/RX NMR field probes for MRI trajectory mapping. , 2016, , .		22
17	Comparison Study of Integrated Potentiostats: Resistive-TIA, Capacitive-TIA, CT $\Delta\Sigma$ Modulator. , 2018, , .		20
18	A 94.3-dB SFDR, 91.5-dB DR, and 200-kS/s CT Incremental $\Delta\Sigma$ Modulator With Differentially Reset FIR Feedback. IEEE Solid-State Circuits Letters, 2019, 2, 87-90.	2.0	20

#	ARTICLE	IF	CITATIONS
19	On the Signal Filtering Property of CT Incremental Sigma-Delta ADCs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1780-1784.	3.0	20
20	A Neuromodulator Frontend With Reconfigurable Class-B Current and Voltage Controlled Stimulator. IEEE Solid-State Circuits Letters, 2018, 1, 54-57.	2.0	17
21	In-depth Analysis and Enhancements of RO-PUFs with a Partial Reconfiguration Framework on Xilinx Zynq-7000 SoC FPGAs. , 2019, , .		17
22	A Nyquist Rate SAR ADC Employing Incremental Sigma Delta DAC Achieving Peak SFDR = 107 dB at 80 kS/s. IEEE Journal of Solid-State Circuits, 2018, 53, 1493-1507.	5.4	14
23	A Chopped Neural Front-End Featuring Input Impedance Boosting With Suppressed Offset-Induced Charge Transfer. IEEE Transactions on Biomedical Circuits and Systems, 2021, 15, 402-411.	4.0	14
24	High-bandwidth floating gate CMOS rectifiers with reduced voltage drop. , 2008, , .		13
25	Towards Low-Cost, High-Sensitivity Point-of-Care Diagnostics Using VCO-Based ESR-on-a-Chip Detectors. IEEE Sensors Journal, 2019, 19, 8995-9003.	4.7	13
26	Fully CMOS integrated active rectifier without voltage drop. , 2008, , .		12
27	Normalization and Multi-Valued Symbol Extraction From RO-PUFs for Enhanced Uniform Probability Distributions. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3372-3376.	3.0	12
28	Experimental results on power efficient single-poly floating gate rectifiers. , 2009, , .		11
29	A Study on self-timed asynchronous subthreshold logic. , 2007, , .		10
30	DISCO - A toolbox for the discrete-time simulation of continuous-time Sigma-Delta modulators using MATLAB. Midwest Symposium on Circuits and Systems, 2007, , .	1.0	10
31	A 0.9-V DAC-Calibration-Free Continuous-Time Incremental Delta-Sigma Modulator Achieving 97-dB SFDR at 2 MS/s in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2022, 57, 3407-3417.	5.4	10
32	A low-power differential common-gate LNA. , 2008, , .		9
33	Calculating transfer functions of CT sigma-delta modulators with arbitrary DAC waveforms. , 2013, , .		9
34	A bidirectional neural interface featuring a tunable recorder and electrode impedance estimation. , 2016, , .		9
35	Integrated Circuit Technology for Next Generation Point-of-Care Spectroscopy Applications. , 2017, 55, 143-151.		9
36	Improved SQNR and MSA in Incremental $\Sigma\Delta$ Modulators by Using a Recuperation Phase. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 557-561.	3.0	9

#	ARTICLE	IF	CITATIONS
37	A 0.4-V $\Delta\Sigma$ Proportional-Integrator-Based Continuous-Time $\Delta\Sigma$ Modulator With 50-dB CMRR. IEEE Journal of Solid-State Circuits, 2018, 53, 3256-3267.	5.4	9
38	An Integrator-Differentiator TIA Using a Multi-Element Pseudo-Resistor in its DC Servo Loop for Enhanced Noise Performance. , 2018, , .		9
39	An Evaluation Study of Various Excitation Signals for Electrical Impedance Spectroscopy. , 2019, , .		9
40	A bidirectional neural interface IC with high voltage compliance and spectral separation. , 2016, , .		8
41	VCO-based ESR-on-a-chip as a tool for low-cost, high-sensitivity food quality control. , 2017, , .		8
42	A 14b, Twofold Time-Interleaved Incremental $\hat{\pi}\hat{\Sigma}$ ADC Using Hardware Sharing. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3681-3692.	5.4	8
43	A Direct Digitizing Chopped Neural Recorder Using a Body-Induced Offset Based DC Servo Loop. IEEE Transactions on Biomedical Circuits and Systems, 2022, 16, 409-418.	4.0	8
44	A comparative study of CMOS LNAs. , 2007, , .		7
45	High efficiency, low-voltage and self-adjusting charge pump with enhanced impedance matching. , 2008, , .		7
46	Evaluation of single-bit sigma-delta modulator DAC for electrical impedance spectroscopy. , 2017, , .		7
47	Input Referred Comparator Noise in SAR ADCs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 718-722.	3.0	7
48	Low-Noise Readout Circuit for an Automotive MEMS Accelerometer. IEEE Open Journal of the Solid-State Circuits Society, 2021, 1, 140-148.	2.7	7
49	Wideband Continuous-Time MASH Delta-Sigma Modulators: A Tutorial Review. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2623-2628.	3.0	7
50	A 0:5V rail-to-rail 1.5 \times W CMOS amplifier for micro-energy harvesting applications. , 2008, , .		5
51	A hexagonal Field Programmable Analog Array consisting of 55 digitally tunable OTAs. , 2008, , .		5
52	A Multilevel Coding Scheme for Multi-Valued Physical Unclonable Functions. IEEE Transactions on Information Forensics and Security, 2021, 16, 3814-3827.	6.9	5
53	Implementation and Analysis of Power Consumption for a Power Optimized Decimator Designed for Cascaded Sigma-Delta A/D Converters. Midwest Symposium on Circuits and Systems, 2006, , .	1.0	4
54	An Unscented Kalman Filter for the estimation of circuit nonidealities with implicit decimation in continuous-time multibit Sigma-Delta modulators. Midwest Symposium on Circuits and Systems, 2007, , .	1.0	4

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55	Estimating Circuit Nonidealities of Continuous-Time Multibit Delta-Sigma Modulators. , 2007, , .		4
56	Design of current reuse CMOS LC-VCO. , 2008, , .		4
57	Optimized scheme for power-of-two coefficient approximation for low power decimation filters in sigma delta ADCs. , 2008, , .		4
58	Systematic approach to the synthesis of continuous-time cascaded sigmaâ€“delta modulators. Analog Integrated Circuits and Signal Processing, 2009, 60, 155-164.	1.4	4
59	Frequency noise of CMOS LC tank oscillators operating in weak inversion. , 2013, , .		4
60	Efficient implementation and stability analysis of a HV-CMOS current/voltage mode stimulator. , 2018, , .		4
61	Noise Analysis of Charge-Balanced Readout Circuits for MEMS Accelerometers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 175-184.	5.4	4
62	Using Polynomial Interpolation for Reproducing Multi-Valued Responses of Physical Unclonable Functions on FPGAs. , 2021, , .		4
63	A PCB-Based 24-Ch. MEA-EIS Allowing Fast Measurement of TEER. IEEE Sensors Journal, 2021, 21, 13048-13059.	4.7	4
64	Time-Continuous Delta-Sigma A/D Converters: From Theory to Practical Implementation. , 2006, , .		3
65	Systematic approach to the synthesis of continuous-time cascaded Sigma-Delta modulators. Midwest Symposium on Circuits and Systems, 2007, , .	1.0	3
66	A Switchable Folded-Cascode OTA without Transmission Gates in the Signal Path. , 2008, , .		3
67	On the Optimization of DT Incremental Sigma-Delta Modulators in Combination with Col Reconstruction Filters. , 2018, , .		3
68	A 94.3-dB SFDR, 91.5-dB DR, and 200-kS/s CT Incremental Deltaâ€“Sigma Modulator With Differentially Reset FIR Feedback. , 2019, , .		3
69	FIR DACs in CT Incremental Delta-Sigma Modulators. , 2020, , .		3
70	Performance Evaluation of Incremental Sigma-Delta ADCs Based on their NTF. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2813-2817.	3.0	3
71	Input Referred Noise of VCO-Based Comparators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 82-86.	3.0	3
72	VCO-based ESR-on-a-chip as a tool for low-cost, high-sensitivity point-of-care diagnostics. , 2017, , .		2

#	ARTICLE	IF	CITATIONS
73	A Low Distortion Continuous Time Sigma Delta Modulator using a High Input Impedance Instrumentation Amplifier for Neural Recording. , 2018, , .		2
74	A 24-Ch. Multi-Electrode Array Allowing Fast EIS to Determine Transepithelial Electrical Resistance. , 2019, , .		2
75	Design Approach for Ring Amplifiers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3444-3457.	5.4	2
76	Efficient High-Resolution Nyquist ADCs. , 2020, , 41-57.		2
77	On the Implicit Anti-Aliasing Feature of Continuous-Time Multistage Noise-Shaping Sigma-Delta Modulators. , 2007, , .		1
78	Analysis of digital gain error compensation in continuous-time cascaded sigma-delta modulators. , 2008, , .		1
79	Comparison of Direct Digitization Current Sensing Circuits for EIS. , 2019, , .		1
80	Comparison of Different Precision Pseudo Resistor Realizations in the DC-Feedback of Capacitive Transimpedance Amplifiers. , 2019, , .		1
81	An Integrator-Differentiator Transimpedance Amplifier Using Tunable Linearized High-Value Multi-Element Pseudo-Resistors. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 3150-3163.	5.4	1
82	A dynamic-Element-Matching architecture using individual element error shaping. , 2008, , .		0
83	Reliability study of single-poly floating gates in 0.13 μm CMOS for use in field programmable analog arrays. , 2008, , .		0
84	Active Integrated Tracking Detectors for MRI-Guided Interventions. Biomedizinische Technik, 2012, 57, .	0.8	0
85	Comparison Study of DAC Realizations in Current Input CTÎ” Modulators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 111-115.	3.0	0
86	Erratum to “A High-Voltage Compliance, 32-Channel Digitally Interfaced Neuromodulation System-on-Chip” IEEE Journal of Solid-State Circuits, 2021, 56, 3203-3203.	5.4	0
87	An Automated Design Environment for CT Incremental Sigma-Delta ADCs. , 2020, , .		0
88	Nonlinearity Modeling for Mixed-Signal Inference Accelerators in Training Frameworks. , 2021, , .		0