

Toshiaki Kirihata

List of Publications by Year in descending order

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69
citing authors

#	ARTICLE	IF	CITATIONS
1	Design Optimization and Modeling of Charge Trap Transistors (CTTs) in 14 nm FinFET Technologies. IEEE Electron Device Letters, 2019, 40, 1100-1103.	3.9	15
2	80-kb Logic Embedded High-K Charge Trap Transistor-Based Multi-Time-Programmable Memory With No Added Process Complexity. IEEE Journal of Solid-State Circuits, 2018, 53, 949-960.	5.4	8
3	14-nm FinFET 1.5 Mb Embedded High-K Charge Trap Transistor One Time Programmable Memory Using Differential Current Sensing. IEEE Solid-State Circuits Letters, 2018, 1, 233-236.	2.0	5
4	A 14 nm 1.1 Mb Embedded DRAM Macro With 1 ns Access. IEEE Journal of Solid-State Circuits, 2016, 51, 230-239.	5.4	17