

Dominik Kasprowicz

List of Publications by Year in descending order

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Version: 2024-02-01

18
papers

114
citations

2682572

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h-index

2053705

5
g-index

18
all docs

18
docs citations

18
times ranked

66
citing authors

#	ARTICLE	IF	CITATIONS
1	Realizing and and or Functions With Single Vertical-Slit Field-Effect Transistor. IEEE Electron Device Letters, 2012, 33, 152-154.	3.9	26
2	CMOS standard cells characterization for defect based testing. , 0, , .		20
3	Is there always performance overhead for regular fabric?. , 2008, , .		14
4	Stacked 3-dimensional 6T SRAM cell with independent double gate transistors. , 2009, , .		13
5	Static Power Consumption in Nano-CMOS Circuits: Physics and Modelling. , 2007, , .		10
6	Improvement of integrated circuit testing reliability by using the defect based approach. Microelectronics Reliability, 2003, 43, 945-953.	1.7	9
7	Adder circuits with transistors using independently controlled gates. , 2009, , .		9
8	Small-signal lumped-element equivalent model for high operating temperature infrared photodetectors. , 2016, , .		4
9	VeSFET as an analog-circuit component. , 2013, , .		2
10	Methods for automated detection of plagiarism in integrated-circuit layouts. Microelectronics Journal, 2014, 45, 1212-1219.	2.0	2
11	Variability-aware table-based DC model of a dual-gate transistor. , 2017, , .		2
12	Table-Based Model of a Dual-Gate Transistor for Statistical Circuit Simulation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1493-1500.	2.7	1
13	Semiconductor Device Parameter Extraction Based on $I_{\text{D}}-V$ Measurements and Simulation. , 2019, , .		1
14	Net-Shape-Based Automated Detection of Integrated-Circuit Layout Plagiarism. Electronics (Switzerland), 2021, 10, 3181.	3.1	1
15	Empirical model of skew in clock-distribution grids. , 0, , .		0
16	CAD tools for analysis of process variability effects in deep submicron CMOS circuits. , 2008, , .		0
17	Foreword to the 17 th IEEE DDECS symposium. , 2014, , .		0
18	Channel charge model of a dual-gate junctionless transistor. , 2015, , .		0