Matteo Repossi

List of Publications by Year
in descending order

27	664	1163117 8	1058476 14
papers	citations	h-index	g-index

28	28	28	730
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Analog Front End of 50-Gb/s SiGe BiCMOS Opto-Electrical Receiver in 3-D-Integrated Silicon Photonics Technology. IEEE Journal of Solid-State Circuits, 2022, 57, 312-322.	5.4	7
2	Multi-Rate Low-Noise Optical Receiver Front-End. Journal of Lightwave Technology, 2020, 38, 4978-4986.	4.6	7
3	12.2 A 4-Channel 200Gb/s PAM-4 BiCMOS Transceiver with Silicon Photonics Front-Ends for Gigabit Ethernet Applications. , 2020, , .		20
4	A 26-Gb/s 3-D-Integrated Silicon Photonic Receiver in BiCMOS-55 nm and PIC25G With â€“ 15.2-dBm OMA Sensitivity. , 2019, , .		0
5	A 26-Gb/s 3-D-Integrated Silicon Photonic Receiver in BiCMOS-55 nm and PIC25G With â˜15.2-dBm OMA Sensitivity. IEEE Solid-State Circuits Letters, 2019, 2, 187-190.	2.0	4
6	Demonstration of a Partially Integrated Silicon Photonics ONU in a Self-Coherent Reflective FDMA PON. Journal of Lightwave Technology, 2017, 35, 1307-1312.	4.6	6
7	23.4 A 56Gb/s 300mW silicon-photonics transmitter in 3D-integrated PIC25G and 55nm BiCMOS technologies. , 2016, , .		18
8	Insights Into Silicon Photonics Machâ€“Zehnder-Based Optical Transmitter Architectures. IEEE Journal of Solid-State Circuits, 2016, 51, 3178-3191.	5.4	32
9	A 25Gb/s 3D-integrated silicon photonics receiver in 65nm CMOS and PIC25G for 100GbE optical links. , 2016, , .		8
10	A fully packaged 25 Gbps/channel WDM photoreceiver module based on a Silicon Photonic Integrated Circuit and a flip-chipped CMOS quad transimpedance amplifier. , 2016, , .		2
11	Transmitter Made up of a Silicon Photonic IC and its Flip-Chipped CMOS IC Driver Targeting Implementation in FDMA-PON. Journal of Lightwave Technology, 2016, 34, 2391-2397.	4.6	6
12	22.9 A 1310nm 3D-integrated silicon photonics Mach-Zehnder-based transmitter with 275mW multistage CMOS driver achieving 6dB extinction ratio at 25Gb/s. , 2015, , .		18
13	A 3D-integrated 25Gbps silicon photonics receiver in PIC25G and 65nm CMOS technologies. , 2014, , .		18
14	A Low-Noise Design Technique for High-Speed CMOS Optical Receivers. IEEE Journal of Solid-State Circuits, 2014, 49, 1437-1447.	5.4	179
15	A 5mW CMOS wideband mm-wave front-end featuring 17dB of conversion gain and 6.5 dB minimum NF. , 2012, , .		1
16	A 25Gb/s low noise 65nm CMOS receiver tailored to 100GBASE-LR4. , 2012, , .		2
17	A 24 GHz Subharmonic Direct Conversion Receiver in 65 nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 88-97.	5.4	38
18	A Wideband Receiver for Multi-Gbit/s Communications in 65 nm CMOS. IEEE Journal of Solid-State Circuits, 2011, 46, 551-561.	5.4	64

#	Article	IF	Citations
19	A 60GHz receiver with 13GHz bandwidth for Gbit/s wireless links in 65nm CMOS. , 2010, , .		2
20	A 12Gb/s 39dB loss-recovery unclocked-DFE receiver with bi-dimensional equalization. , 2010, , .		3
21	A wideband mm-Wave CMOS receiver for Gb/s communications employing interstage coupled resonators. , 2010, , .		37
22	A Multi-Standard 1.5 to 10 Gb/s Latch-Based 3-Tap DFE Receiver With a SSC Tolerant CDR for Serial Backplane Communication. IEEE Journal of Solid-State Circuits, 2009, 44, 1306-1315.	5.4	41
23	Design of Low-Loss Transmission Lines in Scaled CMOS by Accurate Electromagnetic Simulations. IEEE Journal of Solid-State Circuits, 2009, 44, 2605-2615.	5.4	51
24	A 24GHz Sub-Harmonic Receiver Front-End with Integrated Multi-Phase LO Generation in 65nm CMOS. , 2008, , .		20
25	A 3.2-to-7.3GHz Quadrature Oscillator with Magnetic Tuning. Digest of Technical Papers - IEEE International Solid-State Circuits Conference, 2007, , .	0.0	14
26	A Magnetically Tuned Quadrature Oscillator. IEEE Journal of Solid-State Circuits, 2007, 42, 2870-2877.	5.4	61
27	Planar Models of Reconfigurable MEMS Circuits. IEEE Transactions on Microwave Theory and Techniques, 2007, 55, 722-728.	4.6	5