Yifu Gong

List of Publications by Year
in descending order

		1306789	1125271
38 papers	**212** citations	**7** h-index	**13** g-index
38 all docs	**38** docs citations	**38** times ranked	**166** citing authors

#	ARTICLE	IF	CITATIONS
1	Ultra-Low Voltage Split-Data-Aware Embedded SRAM for Mobile Video Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 883-887.	2.2	34
2	Mitigating Nonlinear Effect of Memristive Synaptic Device for Neuromorphic Computing. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 377-387.	2.7	27
3	Low power and high performance dynamic CMOS XOR/XNOR gate design. Microelectronic Engineering, 2011, 88, 2781-2784.	1.1	21
4	Sizing-priority based low-power embedded memory for mobile video applications. , 2016, , .		12
5	Data-Pattern Enabled Self-Recovery Low-Power Storage System for Big Video Data. IEEE Transactions on Big Data, 2019, 5, 95-105.	4.4	12
6	Viewer-Aware Intelligent Efficient Mobile Video Embedded Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 684-696.	2.1	9
7	Variation Aware Sleep Vector Selection in Dual $m V_{m t}$ Dynamic OR Circuits for Low Leakage Register File Design. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 1970-1983.	3.5	8
8	TM-RF: Aging-Aware Power-Efficient Register File Design for Modern Microprocessors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1196-1209.	2.1	8
9	Content-Adaptive Memory for Viewer-Aware Energy-Quality Scalable Mobile Video Systems. IEEE Access, 2019, 7, 47479-47493.	2.6	8
10	SPIDER: Sizing-Priority-Based Application-Driven Memory for Mobile Video Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2625-2634.	2.1	7
11	Linear Optimization for Memristive Device in Neuromorphic Hardware. , 2019, , .		7
12	On Mathematical Models of Optimal Video Memory Design. IEEE Transactions on Circuits and Systems for Video Technology, 2020, 30, 256-266.	5.6	7
13	Data-Driven Intelligent Efficient Synaptic Storage for Deep Learning. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1412-1416.	2.2	6
14	Memory Optimization for Energy-Efficient Differentially Private Deep Learning. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 307-316.	2.1	6
15	Run-Time Deep Learning Enhanced Fast Coding Unit Decision for High Efficiency Video Coding. Journal of Circuits, Systems and Computers, 2020, 29, 2050046.	1.0	5
16	VCAS: Viewing context aware power-efficient mobile video embedded memory. , 2015, , .		4
17	RF-powered battery-less Wireless Sensor Network. , 2016, , .		4
18	Flexible Low-Cost Power-Efficient Video Memory With ECC-Adaptation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1693-1706.	2.1	4

#	Article	IF	Citations
19	Luminance-adaptive smart video storage system. , 2016, , .		4
20	Data-Pattern enabled Self-Recovery multimedia storage system for near-threshold computing. , 2016, , .		3
21	PNS-FCR: Flexible Charge Recycling Dynamic Circuit Technique for Low-Power Microprocessors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 613-624.	2.1	3
22	Application-Aware Quality-Energy Optimization: Mathematical Models Enabled Simultaneous Quality and Energy-Sensitive Optimal Memory Design. IEEE Transactions on Sustainable Computing, 2021, 6, 559-571.	2.2	3
23	Dummy TSV based bit-line optimization in 3D on-chip memory. , 2016, , .		2
24	MTJ based data restoration in non-volatile SRAM. , 2016, , .		2
25	Content-Adaptable ROI-Aware Video Storage for Power-Quality Scalable Mobile Streaming. IEEE Access, 2022, 10, 26830-26848.	2.6	2
26	Analysis and design of CMOS charge pump for EEPROM. , 2014, , .		1
27	A thermal-aware distribution method of TSV in 3D IC. , 2015, , .		1
28	On-chip thermal management method based on phase change material. , 2017, , .		1
29	A Novel Hybrid Delay Unit Based on Dummy TSVs for 3-D On-Chip Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1277-1289.	2.1	1
30	Novel bidirectional IO multiplexing circuit design. , 2014, , .		0
31	Novel local bit line design based on forced-keeper technique for on-chip memories. , 2014, , .		0
32	Novel CMOS SRAM voltage latched sense amplifiers design based on 65 nm technology. , 2014, , .		0
33	Novel CMOS technology compatible nonvolatile on-chip hybrid memory. , 2015, , .		0
34	DCPG: Double-control power gating technique for a 28 nm Cortexâ"¢-A9 MPCore Quad-core processor. , 2015, , .		0
35	Reusable IO technique for improved utility of IC test circuit area. , 2015, , .		0
36	3D memory design based on through silicon vias enabled timing optimization. , 2016, , .		0

#	ARTICLE	IF	CITATIONS
37	Platform design for compatible semi-custom design flow. , 2016, , .		0
38	Closed form delay models for buffer-driven TSVs in 3D on-chip memory. , 2017, , .		0