Alessandro Sottocornola Spinelli

List of Publications by Year
in descending order

168 papers	3,956 citations	136885 32 h-index	168321 53 g-index
168 all docs	168 docs citations	168 times ranked	2132 citing authors

#	Article	IF	Citations
1	Comprehensive Analysis of Random Telegraph Noise Instability and Its Scaling in Decaâ€“Nanometer Flash Memories. IEEE Transactions on Electron Devices, 2009, 56, 1746-1752.	1.6	262
2	Learning of spatiotemporal patterns in a spiking neural network with resistive switching synapses. Science Advances, 2018, 4, eaat4752.	4.7	213
3	Physics and numerical simulation of single photon avalanche diodes. IEEE Transactions on Electron Devices, 1997, 44, 1931-1943.	1.6	148
4	Reviewing the Evolution of the NAND Flash Technology. Proceedings of the IEEE, 2017, 105, 1609-1633.	16.4	135
5	Statistical Model for Random Telegraph Noise in Flash Memories. IEEE Transactions on Electron Devices, 2008, 55, 388-395.	1.6	113
6	Modeling of SILC based on electron and hole tunneling. II. Steady-state. IEEE Transactions on Electron Devices, 2000, 47, 1266-1272.	1.6	99
7	Modeling of SILC based on electron and hole tunneling. I. Transient effects. IEEE Transactions on Electron Devices, 2000, 47, 1258-1265.	1.6	91
8	Random Telegraph Noise Effect on the Programmed Threshold-Voltage Distribution of Flash Memories. IEEE Electron Device Letters, 2009, 30, 984-986.	2.2	85
9	Ultimate Accuracy for the nand Flash Program Algorithm Due to the Electron Injection Statistics. IEEE Transactions on Electron Devices, 2008, 55, 2695-2702.	1.6	66
10	Reliability of NAND Flash Memories: Planar Cells and Emerging Issues in 3D Devices. Computers, 2017, 6, 16.	2.1	66
11	Analytical Model for the Electron-Injection Statistics During Programming of Nanoscale nand Flash Memories. IEEE Transactions on Electron Devices, 2008, 55, 3192-3199.	1.6	62
12	Scaling trends for random telegraph noise in deca-nanometer Flash memories. , 2008, , .		61
13	Theory of direct tunneling current in metalâ€“oxideâ€“semiconductor structures. Journal of Applied Physics, 2002, 91, 1400-1409.	1.1	60
14	A statistical model for SILC in flash memories. IEEE Transactions on Electron Devices, 2002, 49, 1955-1961.	1.6	59
15	Self-consistent 2-D model for quantum effects in n-MOS transistors. IEEE Transactions on Electron Devices, 1998, 45, 1342-1349.	1.6	57
16	Counting photoelectrons in the response of a photomultiplier tube to single picosecond light pulses. Review of Scientific Instruments, 2004, 75, 2762-2765.	0.6	56
17	Mean gain of avalanche photodiodes in a dead space model. IEEE Transactions on Electron Devices, 1996, 43, 23-30.	1.6	55
18	Characterization and Modeling of Temperature Effects in 3-D NAND Flash Arraysâ€”Part I: Polysilicon-Induced Variability. IEEE Transactions on Electron Devices, 2018, 65, 3199-3206.	1.6	52

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19	Photonâ€assisted avalanche spreading in reachâ€through photodiodes. Applied Physics Letters, 1993, 62, 606-608.	1.5	50
20	Carrier quantization at flat bands in MOS devices. IEEE Transactions on Electron Devices, 1999, 46, 383-387.	1.6	50
21	First evidence for injection statistics accuracy limitations in NAND Flash constant-current Fowler-Nordheim programming. , 2007, , .		50
22	Cycling Effect on the Random Telegraph Noise Instabilities of nor and nand Flash Arrays. IEEE Electron Device Letters, 2008, 29, 941-943.	2.2	50
23	Temperature Effects in NAND Flash Memories: A Comparison Between 2-D and 3-D Arrays. IEEE Electron Device Letters, 2017, 38, 461-464.	2.2	50
24	Reliability of NAND Flash Arrays: A Review of What the 2-Dâ€“toâ€“3-D Transition Meant. IEEE Transactions on Electron Devices, 2019, 66, 4504-4516.	1.6	49
25	Threshold-Voltage Instability Due to Damage Recovery in Nanoscale NAND Flash Memories. IEEE Transactions on Electron Devices, 2011, 58, 2406-2414.	1.6	46
26	Origins of 1/f² scaling in the power spectrum of intracortical local field potential. Journal of Neurophysiology, 2012, 107, 984-994.	0.9	46
27	Comprehensive investigation of the impact of lateral charge migration on retention performance of planar and 3D SONOS devices. Solid-State Electronics, 2012, 74, 64-70.	0.8	45
28	Polysilicon quantization effects on the electrical properties of MOS transistors. IEEE Transactions on Electron Devices, 2000, 47, 2366-2371.	1.6	40
29	Stochastic Learning in Neuromorphic Hardware via Spike Timing Dependent Plasticity With RRAM Synapses. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 77-85.	2.7	39
30	Avalanche detector with ultraclean response for time-resolved photon counting. IEEE Journal of Quantum Electronics, 1998, 34, 817-821.	1.0	38
31	Dead space approximation for impact ionization in silicon. Applied Physics Letters, 1996, 69, 3707-3709.	1.5	36
32	A new two-trap tunneling model for the anomalous stress-induced leakage current (SILC) in Flash memories. Microelectronic Engineering, 2001, 59, 189-195.	1.1	36
33	Two-dimensional quantum effects in nanoscale MOSFETs. IEEE Transactions on Electron Devices, 2002, 49, 25-31.	1.6	36
34	Modeling of Tunneling P/E for Nanocrystal Memories. IEEE Transactions on Electron Devices, 2005, 52, 569-576.	1.6	36
35	Physical modeling of single-trap RTS statistical distribution in flash memories. , 2008, , .		35
36	Investigation of the RTN Distribution of Nanoscale MOS Devices From Subthreshold to On-State. IEEE Electron Device Letters, 2013, 34, 683-685.	2.2	35

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37	A simple method for efficient spike detection in multiunit recordings. Journal of Neuroscience Methods, 2007, 163, 176-180.	1.3	30
38	Recent developments on Flash memory reliability. Microelectronic Engineering, 2005, 80, 321-328.	1.1	29
39	Investigation of the Random Telegraph Noise Instability in Scaled Flash Memory Arrays. Japanese Journal of Applied Physics, 2008, 47, 2598-2601.	0.8	29
40	Investigation of the threshold voltage instability after distributed cycling in nanoscale NAND Flash memory arrays. , 2010, , .		29
41	Semi-Analytical Model for the Transient Operation of Gate-All-Around Charge-Trap Memories. IEEE Transactions on Electron Devices, 2011, 58, 3116-3123.	1.6	29
42	Experimental method for the determination of the energy distribution of stress-induced oxide traps. IEEE Electron Device Letters, 1999, 20, 106-108.	2.2	28
43	Accuracy and Issues of the Spectroscopic Analysis of RTN Traps in Nanoscale MOSFETs. IEEE Transactions on Electron Devices, 2013, 60, 833-839.	1.6	28
44	Defects spectroscopy in SiO2 by statistical random telegraph noise analysis. , 2006, , .		27
45	Comparison of Modeling Approaches for the Capacitanceâ€“Voltage and Currentâ€“Voltage Characteristics of Advanced Gate Stacks. IEEE Transactions on Electron Devices, 2007, 54, 106-114.	1.6	27
46	Equivalent cell approach for extraction of the SILC distribution in flash EEPROM cells. IEEE Electron Device Letters, 2002, 23, 40-42.	2.2	26
47	Physical Modeling for Programming of TANOS Memories in the Fowlerâ€“Nordheim Regime. IEEE Transactions on Electron Devices, 2009, 56, 2008-2015.	1.6	26
48	Comprehensive Investigation of Statistical Effects in Nitride Memoriesâ€”Part I: Physics-Based Modeling. IEEE Transactions on Electron Devices, 2010, 57, 2116-2123.	1.6	25
49	Characterization and Modeling of Temperature Effects in 3-D NAND Flash Arraysâ€”Part II: Random Telegraph Noise. IEEE Transactions on Electron Devices, 2018, 65, 3207-3213.	1.6	25
50	A Semi-Analytical Model for Macaroni MOSFETs With Application to Vertical Flash Memories. IEEE Transactions on Electron Devices, 2016, 63, 1871-1876.	1.6	23
51	Investigation and Compact Modeling of the Time Dynamics of the GIDL-Assisted Increase of the String Potential in 3-D NAND Flash Arrays. IEEE Transactions on Electron Devices, 2018, 65, 2804-2811.	1.6	23
52	Three-Dimensional Electrostatics- and Atomistic Doping-Induced Variability of RTN Time Constants in Nanoscale MOS Devicesâ€”Part II: Spectroscopic Implications. IEEE Transactions on Electron Devices, 2012, 59, 2495-2500.	1.6	22
53	Revisiting Charge Trapping/Detrapping in Flash Memories From a Discrete and Statistical Standpointâ€”Part I: (V_{T}) Instabilities. IEEE Transactions on Electron Devices, 2014, 61, 2802-2810.	1.6	22
54	Working Principles of a DRAM Cell Based on Gated-Thyristor Bistability. IEEE Electron Device Letters, 2014, 35, 921-923.	2.2	22

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55	Laser-based calibration for the HARP time of flight system. IEEE Transactions on Nuclear Science, 2003, 50, 1053-1058.	1.2	20
56	A study of hot-hole injection during programming drain disturb in flash memories. IEEE Transactions on Electron Devices, 2006, 53, 668-676.	1.6	20
57	A power-efficient analog integrated circuit for amplification and detection of neural signals. , 2008, 2008, 4911-5.		19
58	A multi-channel low-power system-on-chip for single-unit recording and narrowband wireless transmission of neural signal. , 2010, 2010, 1555-60.		19
59	Three-Dimensional Electrostatics- and Atomistic Doping-Induced Variability of RTN Time Constants in Nanoscale MOS Devicesâ€"Part I: Physical Investigation. IEEE Transactions on Electron Devices, 2012, 59, 2488-2494.	1.6	19
60	Resolving discrete emission events: A new perspective for detrapping investigation in NAND Flash memories. , 2013, , .		19
61	Revisiting Charge Trapping/Detrapping in Flash Memories From a Discrete and Statistical Standpointâ€"Part II: On-Field Operation and Distributed-Cycling Effects. IEEE Transactions on Electron Devices, 2014, 61, 2811-2819.	1.6	19
62	Impact of Cycling on Random Telegraph Noise in 3-D NAND Flash Arrays. IEEE Electron Device Letters, 2018, 39, 1175-1178.	2.2	19
63	Three-Dimensional Simulation of Charge-Trap Memory Programmingâ€"Part I: Average Behavior. IEEE Transactions on Electron Devices, 2011, 58, 1864-1871.	1.6	18
64	Optimization of Threshold Voltage Window Under Tunneling Program/Erase in Nanocrystal Memories. IEEE Transactions on Electron Devices, 2005, 52, 2473-2481.	1.6	17
65	Experimental Study of Data Retention in Nitride Memories by Temperature and Field Acceleration. IEEE Electron Device Letters, 2007, 28, 628-630.	2.2	17
66	Separation of electron and hole traps by transient current analysis. Microelectronic Engineering, 1999, 48, 151-154.	1.1	16
67	Defect Generation Statistics in Thin Gate Oxides. IEEE Transactions on Electron Devices, 2004, 51, 1288-1295.	1.6	16
68	Fitting Cells Into a Narrow <inline-formula> <tex-math notation="LaTeX">V_{T} </tex-math></inline-formula> Interval: Physical Constraints Along the Lifetime of an Extremely Scaled NAND Flash Memory Array. IEEE Transactions on Electron Devices, 2015, 62, 1491-1497.	1.6	16
69	Experimental evidence for recombination-assisted leakage in thin oxides. Applied Physics Letters, 2000, 76, 1719-1721.	1.5	15
70	Statistical Investigation of Random Telegraph Noise ID Instabilities in Flash Cells at Different Initial Trap-filling Conditions. , 2007, , .		15
71	A Compact Multichannel System for Acquisition and Processing of Neural Signals. Annual International Conference of the IEEE Engineering in Medicine and Biology Society, 2007, 2007, 441-4.	0.5	15
72	Avalanche transients in shallow pâ€n junctions biased above breakdown. Applied Physics Letters, 1995, 67, 2627-2629.	1.5	14

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73	Modeling of anomalous SILC in flash memories based on tunneling at multiple defects. Solid-State Electronics, 2002, 46, 1749-1756.	0.8	14
74	Photon time-of-flight distributions through turbid media directly measured with single-photon avalanche diodes. Journal of the Optical Society of America B: Optical Physics, 2003, 20, 2383.	0.9	14
75	A new channel percolation model for V/sub T/ shift in discrete-trap memories. , 0, , .		14
76	RTN ${f V}_{{f T}}$ Instability From the Stationary Trap-Filling Condition: An Analytical Spectroscopic Investigation. IEEE Transactions on Electron Devices, 2008, 55, 655-661.	1.6	14
77	Fundamental Limitations to the Width of the Programmed <formula formulatype="inline"><tex Notation="TeX"> V_{T}</tex></formula> Distribution of <emphasis emphasistype="smcaps">nor</emphasis> Flash Memories. IEEE Transactions on Electron Devices, 2010, 57, 1761-1767.	1.6	14
78	Comprehensive Investigation of Statistical Effects in Nitride Memoriesâ€”Part II: Scaling Analysis and Impact on Device Performance. IEEE Transactions on Electron Devices, 2010, 57, 2124-2131.	1.6	14
79	Compact Modeling of Variability Effects in Nanoscale nand Flash Memories. IEEE Transactions on Electron Devices, 2011, 58, 2302-2309.	1.6	14
80	Variability Effects in Nanowire and Macaroni MOSFETsâ€”Part I: Random Dopant Fluctuations. IEEE Transactions on Electron Devices, 2020, 67, 1485-1491.	1.6	14
81	3D Monte Carlo simulation of the programming dynamics and their statistical variability in nanoscale charge-trap memories. , 2010, , .		13
82	Effect of Floating-Gate Polysilicon Depletion on the Erase Efficiency of nand Flash Memories. IEEE Electron Device Letters, 2010, 31, 647-649.	2.2	13
83	Unsupervised Learning by Spike-Timing-Dependent Plasticity in a Mainstream NOR Flash Memory Arrayâ€”Part I: Cell Operation. IEEE Transactions on Electron Devices, 2019, 66, 4727-4732.	1.6	13
84	Compact modeling of GIDL-assisted erase in 3-D NAND Flash strings. Journal of Computational Electronics, 2019, 18, 561-568.	1.3	13
85	MOSFET simulation with quantum effects and nonlocal mobility model. IEEE Electron Device Letters, 1999, 20, 298-300.	2.2	12
86	A low-power integrated circuit for analog spike detection and sorting in neural prosthesis systems. , 2008, , .		12
87	Variability effects on the V<inf>T</inf> distribution of nanoscale NAND Flash memories. , 2010, , .		12
88	Dynamic Analysis of Current-Voltage Characteristics of Nanoscale Gated-Thyristors. IEEE Electron Device Letters, 2013, 34, 629-631.	2.2	12
89	Cycling pattern and read/bake conditions dependence of random telegraph noise in decananometer NAND flash arrays. , 2015, , .		12
90	Statistical profiling of SILC spot in flash memories. IEEE Transactions on Electron Devices, 2002, 49, 1723-1728.	1.6	11

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91	Fabrication and Characterization of Directly-Assembled ZnO Nanowire Field Effect Transistors with Polymer Gate Dielectrics. Journal of Nanoscience and Nanotechnology, 2007, 7, 4101-4105.	0.9	11
92	Data Retention and Program/Erase Sensitivity to the Array Background Pattern in Deca-nanometer nand Flash Memories. IEEE Transactions on Electron Devices, 2010, 57, 321-327.	1.6	11
93	Reliability constraints for TANOS memories due to alumina trapping and leakage. , 2010, , .		11
94	Impact of atomistic doping and 3D electrostatics on the variability of RTN time constants in flash memories. , 2011, , .		11
95	Characterization and Modeling of Current Transport in Metal/Ferroelectric/Semiconductor Tunnel Junctions. IEEE Transactions on Electron Devices, 2020, 67, 3729-3735.	1.6	11
96	A recombination- and trap-assisted tunneling model for stress-induced leakage current. Solid-State Electronics, 2001, 45, 1361-1369.	0.8	10
97	Optimization of the Nonoverlap Length in Decanano MOS Devices with 2-D QM Simulations. IEEE Transactions on Electron Devices, 2004, 51, 1849-1855.	1.6	10
98	A new physics-based model for TANOS memories program/erase. , 2008, , .		10
99	Investigation of the Turn-ON of T-RAM Cells Under Transient Conditions. IEEE Transactions on Electron Devices, 2015, 62, 1170-1176.	1.6	10
100	Modeling of Dynamic Operation of T-RAM Cells. IEEE Transactions on Electron Devices, 2015, 62, 1905-1911.	1.6	10
101	A detailed investigation of the quantum yield experiment. IEEE Transactions on Electron Devices, 2001, 48, 1696-1702.	1.6	9
102	An analytical model for flat-band polysilicon quantization in MOS devices. IEEE Transactions on Electron Devices, 2002, 49, 1314-1316.	1.6	9
103	Impact of Correlated Generation of Oxide Defects on SILC and Breakdown Distributions. IEEE Transactions on Electron Devices, 2004, 51, 1281-1287.	1.6	9
104	Assessment of distributed-cycling schemes on 45nm NOR flash memory arrays. , 2012, , .		9
105	First Detection of Single-Electron Charging of the Floating Gate of NAND Flash Memory Cells. IEEE Electron Device Letters, 2015, 36, 132-134.	2.2	9
106	Unsupervised Learning by Spike-Timing- Dependent Plasticity in a Mainstream NOR Flash Memory Arrayâ€"Part II: Array Learning. IEEE Transactions on Electron Devices, 2019, 66, 4733-4738.	1.6	9
107	Random Telegraph Noise Intensification After High-Temperature Phases in 3-D NAND Flash Arrays. IEEE Electron Device Letters, 2022, 43, 557-560.	2.2	9
108	An improved formula for the determination of the polysilicon doping. IEEE Electron Device Letters, 2001, 22, 281-283.	2.2	8

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109	Electrical characterization and quantum modeling of MOS capacitors with ultra-thin oxides (1.4â€“3) Tj ETQq1 1 0.784314 rgBT /Ove	0.9	8
110	Detection of nondelayed photons in the forward-scattering of picosecond pulses. Applied Physics Letters, 2004, 84, 2457-2459.	1.5	8
111	Study of nanocrystal memory reliability by CAST structures. Solid-State Electronics, 2004, 48, 1497-1502.	0.8	8
112	Threshold-Voltage statistics and conduction regimes in nanocrystal memories. IEEE Electron Device Letters, 2006, 27, 409-411.	2.2	8
113	Statistical constraints in nanocrystal memory scaling. Microelectronic Engineering, 2007, 84, 2869-2874.	1.1	8
114	Three-Dimensional Simulation of Charge-Trap Memory Programmingâ€”Part II: Variability. IEEE Transactions on Electron Devices, 2011, 58, 1872-1878.	1.6	8
115	Investigation of the programming accuracy of a double-verify ISPP algorithm for nanoscale NAND Flash memories. , 2011, , .		8
116	Quantum-Mechanical Charge Distribution in Cylindrical Gate-All-Around MOS Devices. IEEE Transactions on Electron Devices, 2012, 59, 1837-1843.	1.6	8
117	A new spectral approach to modeling charge trapping/detrapping in NAND Flash memories. , 2014, , .		8
118	Analysis of space and energy distribution of stress-induced oxide traps. Microelectronics Reliability, 1999, 39, 215-219.	0.9	7
119	A Comparative Study of Characterization Techniques for Oxide Reliability in Flash Memories. IEEE Transactions on Device and Materials Reliability, 2004, 4, 320-326.	1.5	7
120	Characterization of oxide trap energy by analysis of the SILC roll-off regime in flash memories. IEEE Transactions on Electron Devices, 2006, 53, 126-134.	1.6	7
121	Temperature dependence of transient and steady-state gate currents in HfO2 capacitors. Applied Physics Letters, 2006, 89, 103504.	1.5	7
122	Comprehensive numerical simulation of threshold-voltage transients in nitride memories. Solid-State Electronics, 2011, 56, 23-30.	0.8	7
123	String Current in Decananometer nand Flash Arrays: A Compact-Modeling Investigation. IEEE Transactions on Electron Devices, 2012, 59, 2331-2337.	1.6	7
124	Random Telegraph Noise in 3D NAND Flash Memories. Micromachines, 2021, 12, 703.	1.4	7
125	Simulation of polysilicon quantization and its effect on n- and p-MOSFET performance. Solid-State Electronics, 2002, 46, 423-428.	0.8	6
126	Improving Floating-Gate Memory Reliability by Nanocrystal Storage and Pulsed Tunnel Programming. IEEE Transactions on Device and Materials Reliability, 2004, 4, 390-396.	1.5	6

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127	Impact of Control-Gate and Floating-Gate Design on the Electron-Injection Spread of Decananometer nand Flash Memories. IEEE Electron Device Letters, 2010, , .	2.2	6
128	Impact of Neutral Threshold-Voltage Spread and Electron-Emission Statistics on Data Retention of Nanoscale nand Flash. IEEE Electron Device Letters, 2010, , .	2.2	6
129	Reliability Characterization Issues for Nanoscale Flash Memories: A Case Study on 45-nm NOR Devices. IEEE Transactions on Device and Materials Reliability, 2013, 13, 362-369.	1.5	6
130	Impact ionization in silicon: A microscopic view. Journal of Applied Physics, 1998, 83, 4760-4764.	1.1	5
131	Edge and percolation effects on VT window in nanocrystal memories. Microelectronic Engineering, 2005, 80, 186-189.	1.1	5
132	An integrated low-noise multichannel system for neural signals amplification. Solid-State Circuits Conference, 2008 ESSCIRC 2008 34th European, 2007, , .	0.0	5
133	Granular electron injection and random telegraph noise impact on the programming accuracy of NOR Flash memories. , 2009, , .		5
134	Reliability investigation of T-RAM cells for DRAM applications. , 2014, , .		5
135	Variability Effects in Nanowire and Macaroni MOSFETsâ€”Part II: Random Telegraph Noise. IEEE Transactions on Electron Devices, 2020, 67, 1492-1497.	1.6	5
136	A comparison of modeling approaches for current transport in polysilicon-channel nanowire and macaroni GAA MOSFETs. Journal of Computational Electronics, 2021, 20, 537-544.	1.3	5
137	A recombination model for transient and stationary stress-induced leakage current. Microelectronics Reliability, 2000, 40, 703-706.	0.9	4
138	Different types of defects in silicon dioxide characterized by their transient behavior. Journal of Applied Physics, 2001, 89, 4189-4191.	1.1	4
139	Modeling of stress-induced leakage current and impact ionization in MOS devices. Solid-State Electronics, 2002, 46, 417-422.	0.8	4
140	Statistical analysis of nanocrystal memory reliability. , 0, , .		4
141	Extraction of the floating-gate capacitive couplings for drain turn-on estimation in discrete-trap memories. Microelectronic Engineering, 2006, 83, 319-322.	1.1	4
142	A wireless microsystem with digital data compression for neural spike recording. Microelectronic Engineering, 2011, 88, 1672-1675.	1.1	4
143	Charge retention phenomena in CT silicon nitride: Impact of technology and operating conditions. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2011, 29, 01AE01.	0.6	4
144	Evidence for an atomistic-doping induced variability of the band-to-band leakage current of nanoscale device junctions. , 2012, , .		4

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145	A step ahead toward a new microscopic picture for charge trapping/detrapping in flash memories. , 2016, , .		4
146	Random Dopant Fluctuation and Random Telegraph Noise in Nanowire and Macaroni MOSFETs. , 2018, , .		4
147	Effect of N2O nitridation on the electrical properties of MOS gate oxides. Microelectronics Reliability, 1998, 38, 239-242.	0.9	3
148	Investigation of the ISPP dynamics and of the programming efficiency of charge-trap memories. , 2010, , .		3
149	Characterization and Modeling of the Band-to-Band Current Variability of Nanoscale Device Junctions. IEEE Transactions on Electron Devices, 2013, 60, 3291-3297.	1.6	3
150	Random Telegraph Noise-Induced Sensitivity of Data Retention to Cell Position in the Programmed Distribution of NAND Flash Memory Arrays. IEEE Electron Device Letters, 2015, 36, 678-680.	2.2	3
151	Investigation of the Program Operation of NAND Flash Cells With a Single-Electron Resolution. IEEE Transactions on Electron Devices, 2016, 63, 2360-2366.	1.6	3
152	Investigation of the Electron-Injection Spread in Barrier-Engineered NAND Flash Memories. IEEE Electron Device Letters, 2009, 30, 769-771.	2.2	2
153	A new erase saturation issue in cylindrical junction-less charge-trap memory arrays. , 2012, , .		2
154	Accelerated reliability testing of flash memory: Accuracy and issues on a 45nm NOR technology. , 2013, , .		2
155	New Erase Constraint for the Junction-Less Charge-Trap Memory Array in Cylindrical Geometry. IEEE Transactions on Electron Devices, 2013, 60, 2203-2208.	1.6	2
156	High-Density Solid-State Storage: A Long Path to Success. , 2021, , .		2
157	Characterization of transient currents in HfO2 capacitors in the short timescale. Microelectronic Engineering, 2006, 83, 1927-1930.	1.1	1
158	Accurate boundary integral calculation in semiconductor device simulation. IEEE Transactions on Electron Devices, 2006, 53, 1730-1733.	1.6	1
159	Transient currents in HfO2 and their impact on circuit and memory applications. , 2006, , .		1
160	A Noise-Resilient Neuromorphic Digit Classifier Based on NOR Flash Memories with Pulseâ€“Width Modulation Scheme. Electronics (Switzerland), 2021, 10, 2784.	1.8	1
161	Introduction to the Special Issue on the 2006 International Reliability Physics Symposium. IEEE Transactions on Device and Materials Reliability, 2007, 7, 50-50.	1.5	0
162	A Multi-Channel Low-Power System-on-Chip for in Vivo Recording and Wireless Transmission of Neural Spikes. Journal of Low Power Electronics and Applications, 2012, 2, 211-241.	1.3	0

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163	Investigation of the RTN amplitude statistics of nanoscale MOS devices by the statistical impedance field method. Journal of Computational Electronics, 2013, 12, 585-591.	1.3	0
164	Assessment of the statistical impedance field method for the analysis of the RTN amplitude in nanoscale MOS devices. , 2013, , .		0
165	Impact of the array background pattern on cycling-induced threshold-voltage instabilities in nanoscale NAND Flash memories. Solid-State Electronics, 2015, 113, 138-143.	0.8	0
166	Comments on â€œA General and Transformable Model Platform for Emerging Multi-Gate MOSFETsâ€• IEEE Electron Device Letters, 2017, 38, 1618-1618.	2.2	0
167	Investigation of the Meyer-Neldel Rule in Si MOSFETs. IEEE Electron Device Letters, 2020, 41, 1821-1824.	2.2	0
168	Random Telegraph Noise in Flash Memories. , 2020, , 201-227.		0