Byeong Yong Kong

List of Publications by Year
in descending order

28	190	1307594 7	1199594 12
papers	citations	h-index	g-index

28	28	28	207
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Area- and Energy-Efficient LDPC Decoder Using Mixed-Resolution Check-Node Processing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 999-1003.	3.0	2
2	A 97-mW Bitwise-Early-Terminating Multiuser Detector for IDMA Systems. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3390-3394.	3.0	2
3	Real-Time SSDLite Object Detection on FPGA. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1192-1205.	3.1	20
4	Low-Latency Polar Decoder Using Overlapped SCL Processing. , 2021, , .		4
5	Bitwise Early Termination of Multiuser Detection for IDMA Systems. IEEE Communications Letters, 2021, 25, 2998-3002.	4.1	4
6	A Low-Latency Multi-Touch Detector Based on Concurrent Processing of Redesigned Overlap Split and Connected Component Analysis. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 166-176.	5.4	8
7	Retrain-Less Weight Quantization for Multiplier-Less Convolutional Neural Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 972-982.	5.4	13
8	A 120-mW 0.16-ms-Latency Connectivity-Scalable Multiuser Detector for Interleave Division Multiple Access. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 470-474.	3.0	3
9	Ultra-Low-Latency LDPC Decoding Architecture using Reweighted Offset Min-Sum Algorithm. , 2020, , .		4
10	Improved Parallel-IDMA Architecture with Low-Complexity Elementary Signal Estimators. , 2020, , .		1
11	Low-Complexity Address Generation for Multiuser Detectors in IDMA Systems. Electronics (Switzerland), 2020, 9, 2069.	3.1	3
12	Multiâ€touch detector architecture based on efficient buffering of intensities and labels. Electronics Letters, 2020, 56, 699-701.	1.0	1
13	Area-Efficient Error Detection Structure for Linear Feedback Shift Registers. Electronics (Switzerland), 2020, 9, 195.	3.1	4
14	Parallel IDMA Architecture Based on Interleaving with Replicated Subpatterns. , 2019, , .		7
15	Efficient Implementation of Multiple Interleavers in IDMA for 5G. , 2018, , .		6
16	Interference Cancellation Architecture for Pipelined Parallel MIMO Detectors. , 2018, , .		1
17	A Memory-Efficient IDMA Architecture Based on On-the-Fly Despreading. IEEE Journal of Solid-State Circuits, 2018, 53, 3327-3337.	5.4	10
18	Hybrid Sorting Architecture for Low-latency Successive Cancellation List Decoding of Polar Codes. Journal of Semiconductor Technology and Science, 2018, 18, 593-601.	0.4	4

#	Article	IF	Citations
19	Improved Sorting Architecture for ${K}$ -Best MIMO Detection. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1042-1046.	3.0	12
20	Low-complexity symbol detection for massive MIMO uplink based on Jacobi method. , 2016, , .		25
21	Fast detection for spatial modulation MIMO based on cost estimation. Electronics Letters, 2016, 52, 671-673.	1.0	0
22	Efficient Sorting Architecture for Successive-Cancellation-List Decoding of Polar Codes. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 673-677.	3.0	32
23	Narrow-range frequency estimation based on comprehensive optimization of DFT and interpolation. , 2015, , .		0
24	Low-Complexity Low-Latency Architecture for Matching of Data Encoded With Hard Systematic Error-Correcting Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1648-1652.	3.1	6
25	Efficient Tree-Traversal Strategy for Soft-Output MIMO Detection Based on Candidate-Set Reorganization. IEEE Communications Letters, 2013, 17, 1758-1761.	4.1	2
26	Hardwareâ€efficient tree expansion for MIMO symbol detection. Electronics Letters, 2013, 49, 226-228.	1.0	3
27	Adaptive Metric Calculation for Improving Detection Capability of MIMO Detectors. , 2013, , .		0
28	FIR Filter Synthesis Based on Interleaved Processing of Coefficient Generation and Multiplier-Block Synthesis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1169-1179.	2.7	13