Bah-Hwee Gwee

List of Publications by Year
in descending order

122 papers	1,143 citations	516215 16 h-index	552369 26 g-index
122 all docs	122 docs citations	122 times ranked	588 citing authors

#	Article	IF	Citations
1	Delayered IC image analysis with templateâ€based Tanimoto Convolution and Morphological Decision. IET Circuits, Devices and Systems, 2022, 16, 169-177.	0.9	3
2	A Highly Secure FPGA-Based Dual-Hiding Asynchronous-Logic AES Accelerator Against Side-Channel Attacks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1144-1157.	2.1	6
3	A Novel Normalized Variance-Based Differential Power Analysis Against Masking Countermeasures. IEEE Transactions on Information Forensics and Security, 2021, 16, 3767-3779.	4.5	3
4	Normalized Differential Power Analysis - for Ghost Peaks Mitigation. , 2021, , .		1
5	Dual-Hiding Side-Channel-Attack Resistant FPGA-Based Asynchronous-Logic AES: Design, Countermeasures and Evaluation. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 343-356.	2.7	13
6	A Power-Aware Toggling-Frequency Actuator in Data-Toggling SRAM for Secure Data Protection. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 2122-2126.	2.2	1
7	Deep learning-based image analysis framework for hardware assurance of digital integrated circuits. Microelectronics Reliability, 2021, 123, 114196.	0.9	13
8	Joint Anomaly Detection and Inpainting for Microscopy Images Via Deep Self-Supervised Learning. , 2021, , .		4
9	ASIC Circuit Netlist Recognition Using Graph Neural Network. , 2021, , .		6
10	A DPA-Resistant Asynchronous-Logic NoC Router with Dual-Supply-Voltage-Scaling for Multicore Cryptographic Applications. , 2020, , .		1
11	A Highly Efficient Power Model for Correlation Power Analysis (CPA) of Pipelined Advanced Encryption Standard (AES). , 2020, , .		5
12	Deep Learning-Based Image Analysis Framework for Hardware Assurance of Digital Integrated Circuits. , 2020, , .		3
13	High Efficiency Early-Complete Brute Force Elimination Method for Security Analysis of Camouflage IC. , 2020, , .		1
14	High Throughput and Secure Authentication-Encryption on Asynchronous Multicore Processor for Edge Computing IoT Applications. , 2020, , .		0
15	A Highly Efficient Side Channel Attack with Profiling through Relevance-Learning on Physical Leakage Information. IEEE Transactions on Dependable and Secure Computing, 2019, 16, 376-387.	3.7	10
16	A Secure Data-Toggling SRAM for Confidential Data Protection. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4186-4199.	3.5	9
17	Low Gate-Count Ultra-Small Area Nano Advanced Encryption Standard (AES) Design. , 2019, , .		12
18	Global Template Projection and Matching Method for Training-Free Analysis of Delayered IC Images. , 2019, , .		9

#	Article	IF	Citations
19	Side-Channel-Attack Resistant Dual-Rail Asynchronous-Logic AES Accelerator Based on Standard Library Cells. , 2019, , .		9
20	Reconfigurable Routing Paths As Noise Generators Using NoC Platform for Hardware Security Applications. , 2019, , .		1
21	A High Throughput and Secure Authentication-Encryption AES-CCM Algorithm on Asynchronous Multicore Processor. IEEE Transactions on Information Forensics and Security, 2019, 14, 1023-1036.	4.5	20
22	A Hierarchical Multiclassifier System for Automated Analysis of Delayered IC Images. IEEE Intelligent Systems, 2019, 34, 36-43.	4.0	14
23	Hybrid <inline-formula> <tex-math notation="LaTeX">${K}$ </tex-math> </inline-formula>-Means Clustering and Support Vector Machine Method for via and Metal Line Detections in Delayered IC Images. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1849-1853.	2.2	18
24	Asynchronous-Logic QDI Quad-Rail Sense-Amplifier Half-Buffer Approach for NoC Router Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 196-200.	2.1	12
25	A Noise-Shaped Randomized Modulation for Switched-Mode DC-DC Converters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 394-405.	3.5	14
26	Deep Learning for Automatic IC Image Analysis. , 2018, , .		23
27	A Comparative Analysis of 65nm CMOS SRAM and Commercial SRAMs in Security Vulnerability Evaluation. , 2018, , .		4
28	DPA-resistant QDI dual-rail AES S-Box based on power-balanced weak-conditioned half-buffer. , 2017, , .		2
29	A low-harmonics low-noise randomized modulation scheme for multi-phase DC-DC converters. , 2017, , .		3
30	Highly secured state-shift local clock circuit to countermeasure against side channel attack. , 2017, , .		7
31	A class-E RF power amplifier with a novel matching network for high-efficiency dynamic load modulation. , 2017, , .		3
32	A Highly-Secured Arithmetic Hiding cum Look-Up Table (AHLUT) based S-Box for AES-128 Implementation. Advances in Science, Technology and Engineering Systems, 2017, 2, 420-426.	0.4	0
33	High performance low overhead template-based Cell-Interleave Pipeline (TCIP) for asynchronous-logic QDI circuits. , 2016, , .		0
34	Interceptive side channel attack on AES-128 wireless communications for IoT applications. , 2016, , .		18
35	Success rate model for fully AES-128 in correlation power analysis. , 2016, , .		7
36	A high-efficiency Class-E polar power-amplifier with a novel digitally-controlled output matching network. , 2016, , .		1

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37	Security analysis of asynchronous-logic QDI cell approach for differential power analysis attack. , 2016, , .		2
38	Highly secured arithmetic hiding based S-Box on AES-128 implementation. , 2016, , .		3
39	Secured Low Power Overhead Compensator Look-Up-Table (LUT) Substitution Box (S-Box) Architecture. , 2016, , .		8
40	Sense Amplifier Half-Buffer (SAHB): A Low-Power High-Performance Asynchronous Logic QDI Cell Template. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, , 1-14.	2.1	7
41	Area-efficient and low stand-by power 1k-byte transmission-gate-based non-imprinting high-speed erase (TNIHE) SRAM. , 2016, , .		6
42	High Secured Low Power Multiplexer-LUT Based AES S-Box Implementation. , 2016, , .		15
43	Low Normalized Energy Derivation Asynchronous Circuit Synthesis Flow through Fork-Join Slack Matching for Cryptographic Applications. , 2016, , .		2
44	High robustness energy- and area-efficient dynamic-voltage-scaling 4-phase 4-rail asynchronous-logic Network-on-Chip (ANoC). , 2015, , .		8
45	Novel real-time system design for floating-point sub-Nyquist multi-coset signal blind reconstruction. , 2015, , .		4
46	Counteracting differential power analysis: Hiding encrypted data from circuit cells. , 2015, , .		12
47	Low power subâ€threshold asynchronous quasiâ€delayâ€insensitive 32â€bit arithmetic and logic unit based on autonomous signalâ€validity halfâ€buffer. IET Circuits, Devices and Systems, 2015, 9, 309-318.	0.9	5
48	A single-V<inf>DD</inf> half-clock-tolerant fine-grained dynamic voltage scaling pipeline. , 2015, , .		0
49	A self-oscillating class D audio amplifier with dual voltage and current feedback. , 2014, , .		2
50	Low delay-variation sub-/near-threshold asynchronous-to-synchronous interface controller for GALS Network-on-Chips. , 2014, , .		2
51	Design of an output stage for high switching frequency DC-DC converters. , 2014, , .		0
52	A Low Overhead Quasi-Delay-Insensitive (QDI) Asynchronous Data Path Synthesis Based on Microcell-Interleaving Genetic Algorithm (MIGA). IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 989-1002.	1.9	11
53	A Randomized Modulation scheme for filterless digital Class D audio amplifiers. , 2014, , .		2
54	Synthesis of asynchronous QDI circuits using synchronous coding specifications. , 2014, , .		2

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55	Ultra-Low Power Read-Decoupled SRAMs with Ultra-Low Write-Bitline Voltage Swing. Circuits, Systems, and Signal Processing, 2014, 33, 3317-3329.	1.2	4
56	A dynamic-voltage-scaling 1kbyte×8-bit non-imprinting Master-Slave SRAM with high speed erase for low-power operation. , 2014, , .		3
57	A dual-core 8051 microcontroller system based on synchronous-logic and asynchronous-logic. , 2013, , .		1
58	Low power sub-threshold asynchronous QDI Static Logic Transistor-level Implementation (SLTI) 32-bit ALU. , 2013, , .		1
59	An Ultra-Low Power Asynchronous-Logic In-Situ Self-Adaptive $V_{m DD}$ System for Wireless Sensor Networks. IEEE Journal of Solid-State Circuits, 2013, 48, 573-586.	3.5	33
60	Designing globally-asynchronous-locally-system from multi-rate Simulink model. , 2013, , .		0
61	Synchronous-Logic and Asynchronous-Logic 8051 Microcontroller Cores for Realizing the Internet of Things: A Comparative Study on Dynamic Voltage Scaling and Variation Effects. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2013, 3, 23-34.	2.7	37
62	Energy-delay efficient asynchronous-logic 16×16-bit pipelined multiplier based on Sense Amplifier-Based Pass Transistor Logic. , 2012, , .		1
63	An Ultra-Dynamic Voltage Scalable (U-DVS) 10T SRAM with bit-interleaving capability. , 2012, , .		5
64	A comparative study on asynchronous Quasi-Delay-Insensitive templates. , 2012, , .		0
65	Extracting functional modules from flattened gate-level netlist. , 2012, , .		12
66	A robust asynchronous approach for realizing ultra-low power digital Self-Adaptive V<inf>DD</inf> Scaling system. , 2012, , .		1
67	Synchronous-Logic and Globally-Asynchronous-Locally-Synchronous (GALS) Acoustic Digital Signal Processors. IEEE Journal of Solid-State Circuits, 2012, 47, 769-780.	3.5	28
68	A power-efficient integrated input/output completion detection circuit for asynchronous-logic quasi-delay-insensitive Pre-Charged Half-Buffer. , 2011, , .		1
69	Improved asynchronous-logic dual-rail Sense Amplifier-based Pass Transistor Logic with high speed and low power operation. , 2011, , .		3
70	Modeling and Synthesis of Asynchronous Pipelines. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 682-695.	2.1	8
71	Asynchronous DSP for low-power energy-efficient embedded systems. Microprocessors and Microsystems, 2011, 35, 318-328.	1.8	3
72	Quasi-delay-insensitive compiler: Automatic synthesis of asynchronous circuits from verilog specifications. , 2011, , .		7

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73	A low-power dual-rail inputs write method for bit-interleaved memory cells. , 2011, , .		1
74	A highly efficient method for extracting FSMs from flattened gate-level netlist. , 2010, , .		47
75	An ultra-low power asynchronous quasi-delay-insensitive (QDI) sub-threshold memory with bit-interleaving and completion detection. , 2010, , .		6
76	An efficient VLSI circuit extraction algorithm for transistor-level to gate-level abstraction. , 2010, , .		0
77	Analytical delay variation modeling for evaluating sub-threshold synchronous/asynchronous designs. , 2010, , .		8
78	A Randomized Wrapped-Around Pulse Position Modulation Scheme for DCâ€“DC Converters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2320-2333.	3.5	26
79	Low Power Asynchronous Circuit Design: An FFT/IFFT Processor. , 2010, , 53-95.		0
80	A Low-Voltage Micropower Asynchronous Multiplier With Shiftâ€“Add Multiplication Approach. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 1349-1359.	3.5	13
81	Spectral Analysis of Randomized Switching Frequency Modulation Scheme with a Triangular Distribution for DC-DC Converters. , 2009, , .		1
82	Fine-grained power gating for leakage and short-circuit power reduction by using asynchronous-logic. , 2009, , .		19
83	A Low-Voltage Micropower Digital Class-D Amplifier Modulator for Hearing Aids. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 337-349.	3.5	19
84	A performance comparison on asynchronous matched-delay templates. , 2009, , .		1
85	Asynchronous Control Network Optimization Using Fast Minimum-Cycle-Time Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 985-998.	1.9	6
86	De-synchronization of a point-of-sales digital-logic controller. , 2008, , .		0
87	A semi-custom memory design for an asynchronous 8051 microcontroller. , 2008, , .		2
88	A Low Energy FFT/IFFT Processor for Hearing Aids. , 2007, , .		3
89	A 32-point FFT based Noise Reduction Algorithm for Single Channel Speech Signals. , 2007, , .		2
90	An Asynchronous Dual-Rail Multiplier based on Energy-Efficient STFB Templates. , 2007, , .		2

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91	A Review of Design Methods for Digital Modulators. , 2007, , .		3
92	Energy-Efficient Synchronous-Logic and Asynchronous-Logic FFT/IFFT Processors. IEEE Journal of Solid-State Circuits, 2007, 42, 2034-2045.	3.5	38
93	Fast and memory-efficient invariant computation of ordinary Petri nets. IET Computers and Digital Techniques, 2007, 1, 612.	0.9	2
94	A Simple Methodology of Designing Asynchronous Circuits Using Commercial IC Design Tools and Standard Library Cells. , 2007, , .		2
95	Design of several asynchronous-logic macrocells for a low-voltage micropower cell library. IET Circuits, Devices and Systems, 2007, 1, 161.	0.9	5
96	Low energy 16-bit Booth leapfrog array multiplier using dynamic adders. IET Circuits, Devices and Systems, 2007, 1, 170.	0.9	11
97	A 16-Channel Low-Power Nonuniform Spaced Filter Bank Core for Digital Hearing Aids. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2006, 53, 853-857.	2.3	45
98	An evolution search algorithm for solving N-queen problems. International Journal of Computer Applications in Technology, 2005, 24, 43.	0.3	4
99	A micropower low-distortion digital class-D amplifier based on an algorithmic pulsewidth modulator. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2005, 52, 2007-2022.	0.1	50
100	A micropower low-voltage multiplier with reduced spurious switching. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2005, 13, 255-265.	2.1	42
101	An investigation into the parameters affecting total harmonic distortion in low-voltage low-power Class-D amplifiers. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2003, 50, 1304-1315.	0.1	41
102	An investigation into the parameters affecting total harmonic distortion in low-voltage low-power class-d amplifiers. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2003, 50, 1304-1315.	0.1	5
103	A micropower low-distortion digital pulsewidth modulator for a digital class D amplifier. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2002, 49, 245-256.	2.3	41
104	A GA with heuristic-based decoder for IC floorplanning. The Integration VLSI Journal, 1999, 28, 157-172.	1.3	31
105	Self-adjusting diagnostic system for the manufacture of crystal resonators. IEEE Transactions on Industry Applications, 1996, 32, 73-79.	3.3	3
106	A GA paradigm for learning fuzzy rules. Fuzzy Sets and Systems, 1996, 82, 177-186.	1.6	74
107	Polyominoes tiling by a genetic algorithm. Computational Optimization and Applications, 1996, 6, 273-291.	0.9	19
108	Intelligent monitoring of a frequency-trimming process. Journal of Intelligent Manufacturing, 1993, 4, 375-383.	4.4	2

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109	A novel sampling process and pulse generator for a low distortion digital pulse-width modulator for digital class D amplifiers. , 0, , .		6
110	Low-voltage micropower asynchronous multiplier for hearing instruments. , 0, , .		6
111	An investigation on the parameters affecting total harmonic distortion in class D amplifiers. , 0, , .		10
112	A novel pulse width modulation sampling process for low power, low distortion digital Class D amplifiers. , 0, , .		1
113	A novel low-power low-voltage Class D amplifier with feedback for improving THD, power efficiency and gain linearity. , 0, , .		21
114	A digital Class D amplifier design embodying a novel sampling process and pulse generator. , 0, , .		6
115	Low-voltage asynchronous adders for low power and high speed applications. , 0, , .		8
116	A low-voltage micropower asynchronous multiplier for a multiplierless FIR filter. , 0, , .		4
117	A novel combined first and second order Lagrange interpolation sampling process for a digital class D amplifier. , 0, , .		2
118	A low power 16-bit Booth Leapfrog array multiplier using Dynamic Adders. , 0, , .		1
119	Low-Voltage Micropower Multipliers with Reduced Spurious Switching. , 0, , .		1
120	A Combined Interpolatorless Interpolation and High Accuracy Sampling Process for Digital Class D Amplifiers. , 0, , .		5
121	A Low-Energy Asynchronous FFT/IFFT Processor for Hearing Aid Applications. , 0, , .		2
122	An Acoustic Noise Suppression System with Reduced Musical Artifacts. , 0, , .		1