Eric Beyne

List of Publications by Year
in descending order

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472	6,164	182225	214428
papers	citations	30 h-index	50 g-index

479	479	479	2611
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	System Optimization: High-Frequency Buck Converter With 3-D In-Package Air-Core Inductor. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2022, 12, 401-409.	1.4	2
2	Heat transfer and pressure drop correlations for direct on-chip microscale jet impingement cooling with alternating feeding and draining jets. International Journal of Heat and Mass Transfer, 2022, 182, 121865.	2.5	7
3	Application of the surface planer process to Cu pillars and wafer support tape for high-coplanarity wafer-level packaging. International Journal of Advanced Manufacturing Technology, 2022, 119, 3427-3435.	1.5	2
4	84%-Efficiency Fully Integrated Voltage Regulator for Computing Systems Enabled by 2.5-D High-Density MIM Capacitor. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 661-665.	2.1	3
5	Reliability Investigation of W2W Hybrid Bonding Interface: Breakdown Voltage and Leakage Mechanism. , 2022, , .		2
6	Fundamental study of IMC grains at low anneal temperature. , 2022, , .		1
7	Carrier Systems for Collective Die-to-Wafer Bonding. , 2022, , .		4
8	Direct Bonding Using Low Temperature SiCN Dielectrics. , 2022, , .		8
9	Low temperature backside damascene processing on temporary carrier wafer targeting 7Î¼m and 5Î¼m pitch microbumps for N equal and greater than 2 die to wafer TCB stacking. , 2022, , .		4
10	Buried Power Rails and Nano-Scale TSV: Technology Boosters for Backside Power Delivery Network and 3D Heterogeneous Integration. , 2022, , .		9
11	Broadband Characterization of Polymers under Reliability Stresses and Impact of Capping Layer. , 2022, , .		1
12	Fine-pitch bonding technology with surface-planarized solder micro-bump/polymer hybrid for 3D integration. Japanese Journal of Applied Physics, 2021, 60, 026502.	0.8	7
13	A Novel Method for Characterization of Ultralow Viscosity NCF Layers Using TCB for 3D Assembly. Journal of Microelectronics and Electronic Packaging, 2021, 18, 12-20.	0.8	0
14	Epitaxial Growth of Active Si on Top of SiGe Etch Stop Layer in View of 3D Device Integration. ECS Journal of Solid State Science and Technology, 2021, 10, 014001.	0.9	2
15	Localization of Electrical Defects in Hybrid Bonding Interconnect Structures by Scanning Photocapacitance Microscopy. IEEE Transactions on Instrumentation and Measurement, 2021, 70, 1-7.	2.4	1
16	Fine-pitch 3D system integration and advanced CMOS nodes: technology and system design perspective. , 2021, , .		2
17	Experimental and Numerical Study of 3-D Printed Direct Jet Impingement Cooling for High-Power, Large Die Size Applications. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2021, 11, 415-425.	1.4	9
18	Characterization of through-silicon vias using laser terahertz emission microscopy. Nature Electronics, 2021, 4, 202-207.	13.1	21

#	Article	IF	Citations
19	Cobalt-Tin Intermetallic Compounds as Alternative Surface Finish for Low Temperature Die-to-Wafer Solder Stacking. , 2021, , .		2
20	Multi-tier $mathrm{N}=4$ Binary Stacking, combining Face-to-Face and Back-to-Back Hybrid Wafer-to-Wafer Bonding Technology. , 2021, , .		5
21	Advances in Photosensitive Polymer Based Damascene RDL Processes: Toward Submicrometer Pitches With More Metal Layers. , 2021, , .		10
22	Acoustic modulation during laser debonding of collective hybrid bonded dies. , 2021, , .		7
23	Broadband permittivity characterization of polymers up to 110GHz using co-planar waveguides. , 2021, , .		2
24	Demonstration of a collective hybrid die-to-wafer integration using glass carrier. , 2021, , .		6
25	Thermal analysis of 3D functional partitioning for high-performance systems. , 2021, , .		3
26	A study on IMC morphology and integration flow for low temperature and high throughput TCB down to $10mu mathrm{m}$ pitch microbumps. , 2021, , .		1
27	Characterization of bonding activation sequences to enable ultra-low Cu/SiCN wafer level hybrid bonding. , 2021, , .		13
28	Reliability Study of Polymers Used in Sub-4-Î¼m Pitch RDL Applications. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2021, 11, 1073-1080.	1.4	11
29	Power from Below: Buried Interconnects Will Help Save Moore's Law. IEEE Spectrum, 2021, 58, 46-51.	0.5	4
30	The unique properties of SiCN as bonding material for hybrid bonding. , 2021, , .		5
31	Design And Sign-off Methodologies For Wafer-To-Wafer Bonded 3D-ICs At Advanced Nodes (invited). , 2021, , .		2
32	3D SoC integration, beyond 2.5D chiplets. , 2021, , .		20
33	Area-Selective Electroless Deposition of Cu for Hybrid Bonding. IEEE Electron Device Letters, 2021, 42, 1826-1829.	2.2	8
34	Experimental and numerical investigation of direct liquid jet impinging cooling using 3D printed manifolds on lidded and lidless packages for 2.5D integrated systems. Applied Thermal Engineering, 2020, 164, 114535.	3.0	24
35	Low-Cost Energy-Efficient On-Chip Hotspot Targeted Microjet Cooling for High- Power Electronics. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 577-589.	1.4	21
36	Entire Domain Basis Function Expansion of the Differential Surface Admittance for Efficient Broadband Characterization of Lossy Interconnects. IEEE Transactions on Microwave Theory and Techniques, 2020, 68, 1217-1233.	2.9	18

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37	A Novel Resistance Measurement Methodology for $In-Situ$ UBM/Solder Interfacial Reaction Monitoring. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 30-38.	1.4	3
38	Power Delivery Network (PDN) Modeling for Backside-PDN Configurations With Buried Power Rails and mu TSVs. IEEE Transactions on Electron Devices, 2020, 67, 11-17.	1.6	21
39	Integrated magnetic cores in FOWLP and their applications. , 2020, , .		0
40	Morphological characterization and mechanical behavior by dicing and thinning on direct bonded Si wafer. Journal of Manufacturing Processes, 2020, 58, 811-818.	2.8	8
41	Photosensitive polymer reliability for fine pitch RDL applications. , 2020, , .		10
42	Nozzle scaling effects for the thermohydraulic performance of microjet impingement cooling with distributed returns. Applied Thermal Engineering, 2020, 180, 115767.	3.0	11
43	Demonstration of a collective hybrid die-to-wafer integration. , 2020, , .		10
44	Optical Beam-Based Defect Localization Methodologies for Open and Short Failures in Micrometer-Scale 3-D TSV Interconnects. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 1542-1551.	1.4	8
45	Introduction of a New Carrier System for Collective Die-to-Wafer Hybrid Bonding and Laser-Assisted Die Transfer. , 2020, , .		11
46	10 and 7 Î¼m Pitch Thermo-compression Solder Joint, Using A Novel Solder Pillar And Metal Spacer Process. , 2020, , .		11
47	A novel iso-thermal intermetallic compound insertion bonding approach to improve throughput for 3D die to wafer stacking. , 2020, , .		4
48	3D Wafer-to-Wafer Bonding Thermal Resistance Comparison: Hybrid Cu/dielectric Bonding versus Dielectric via-last Bonding. , 2020, , .		9
49	Extreme Wafer Thinning and nano-TSV processing for 3D Heterogeneous Integration. , 2020, , .		26
50	Novel Cu/SiCN surface topography control for 1 Î¼m pitch hybrid wafer-to-wafer bonding. , 2020, , .		41
51	Process development and characterization of 3D multi-die stacking. , 2020, , .		0
52	A Novel Intermetallic Compound Insertion Bonding to Improve Throughput for Sequential 3-D Stacking. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 669-678.	1.4	6
53	3D Heterogeneous Package Integration of Air/Magnetic Core Inductor: 89%-Efficiency Buck Converter with Backside Power Delivery Network. , 2020, , .		4
54	Characterization of Silicon Carbon Nitride for Low Temperature Wafer-to-Wafer Direct Bonding. ECS Transactions, 2020, 98, 21-31.	0.3	3

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55	Evaluation of UBM oxidation through air exposure and heating and effectiveness of wet and plasma cleaning on solder joint formation during TCB. , 2020, , .		0
56	System exploration and technology demonstration of 3D Wafer-to-Wafer integrated STT-MRAM based caches for advanced Mobile SoCs. , 2020, , .		6
57	Film Characterization of Low-Temperature Silicon Carbon Nitride for Direct Bonding Applications. ECS Journal of Solid State Science and Technology, 2020, 9, 123011.	0.9	11
58	A novel method for characterization of Ultra Low Viscosity NCF layers using TCB for 3D Assembly. International Symposium on Microelectronics, 2020, 2020, 000185-000191.	0.3	0
59	ELD NiB for microbumps passivation and wirebonding. , 2020, , .		1
60	Tbps/mm bandwidth for chip-to-chip communication using fine pitch damascene RDL. , 2020, , .		1
61	Epitaxial Growth of Active Si on Top of SiGe Etch Stop Layer in View of 3D Device Integration. ECS Transactions, 2020, 98, 157-166.	0.3	0
62	Modeling of Buck Converter with 3D Air-Core Inductor. , 2020, , .		1
63	Defect Identification in Bonding Surface Layers by Positron Annihilation Spectroscopy. , 2019, , .		0
64	Thermal Analysis of a 3D Flip-chip Fan-out Wafer Level Package (fcFOWLP) for High Bandwidth 3D Integration. , 2019, , .		1
65	Effects of isothermal storage on grain structure of Cu/Sn/Cu microbump interconnects for 3D stacking. Microelectronics Reliability, 2019, 102, 113296.	0.9	12
66	Pre-bonding Characterization of SiCN Enabled Wafer Stacking. , 2019, , .		1
67	Influence of Composition of SiCN as Interfacial Layer on Plasma Activated Direct Bonding. ECS Journal of Solid State Science and Technology, 2019, 8, P346-P350.	0.9	31
68	Advanced Dicing Technologies for Combination of Wafer to Wafer and Collective Die to Wafer Direct Bonding. , 2019, , .		11
69	Study of the effect of Sn grain boundaries on IMC morphology in solid state inter-diffusion soldering. Scientific Reports, 2019, 9, 14862.	1.6	11
70	First Demonstration of a Low Cost/Customizable Chip Level 3D Printed Microjet Hotspot-Targeted Cooler for High Power Applications. , 2019, , .		5
71	Advances in Temporary Carrier Technology for High-Density Fan-Out Device Build-up. , 2019, , .		9
72	A Highly Reliable 1.4Î¼m Pitch Via-Last TSV Module for Wafer-to-Wafer Hybrid Bonded 3D-SOC Systems. , 2019, , .		10

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73	Inductive Links for 3D Stacked Chip-to-Chip Communication. , 2019, , .		4
74	Enabling Ultra-Thin Die to Wafer Hybrid Bonding for Future Heterogeneous Integrated Systems. , 2019, , .		21
75	Direct Bonding of low Temperature Heterogeneous Dielectrics. , 2019, , .		11
76	Conjugate Heat Transfer and Fluid Flow Modeling for Liquid Microjet Impingement Cooling with Alternating Feeding and Draining Channels. Fluids, 2019, 4, 145.	0.8	14
77	Study of wafer warpage for Fan-Out wafer level packaging: finite element modelling and experimental validation. , 2019, , .		6
78	Experimental Characterization of a Chip-Level 3-D Printed Microjet Liquid Impingement Cooler for High-Performance Systems. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019, 9, 1815-1824.	1.4	13
79	Experimental characterization and model validation of liquid jet impingement cooling using a high spatial resolution and programmable thermal test chip. Applied Thermal Engineering, 2019, 152, 308-318.	3.0	31
80	Design Enablement of Fine Pitch Face-to-Face 3D System Integration using Die-by-Die Place & Route. , 2019, , .		8
81	Process Complexity and Cost Considerations of Multi-Layer Die Stacks. , 2019, , .		1
82	New approach to apply 1,2,3-benzotriazole as a capping layer on UBMs for 3D TCB stacking and investigation of oxidation protection and solder wetting. , 2019, , .		0
83	RF characterization of mold compound materials and high-Q integrated passives using fan-out wafer-level packaging technology. , 2019, , .		1
84	Protective Layer for Collective Die to Wafer Hybrid Bonding. , 2019, , .		10
85	Novel Temporary Bonding and Debonding Solutions Enabling an Ultrahigh Interonnect Density Fo-Wlp Structure Assembly with Quasi-Zero Die Shift. , 2019, , .		5
86	A High-Bandwidth Fine-Pitch 2.57Tbps/mm In-package Communication Link Achieving 48fJ/bit/mm Efficiency. , 2019, , .		3
87	Modeling Copper Plastic Deformation and Liner Viscoelastic Flow Effects on Performance and Reliability in Through Silicon Via (TSV) Fabrication Processes. IEEE Transactions on Device and Materials Reliability, 2019, 19, 642-653.	1.5	11
88	Thermal Management and Processing Optimization for 3D Multi-layer Stacked ICs. , 2019, , .		2
89	The Growing Application Field of Laser Debonding: From Advanced Packaging to Future Nanoelectronics. , 2019, , .		8
90	In-Line Metrology for Characterization and Control of Extreme Wafer Thinning of Bonded Wafers. IEEE Transactions on Semiconductor Manufacturing, 2019, 32, 54-61.	1.4	7

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91	High-Efficiency Polymer-Based Direct Multi-Jet Impingement Cooling Solution for High-Power Devices. IEEE Transactions on Power Electronics, 2019, 34, 6601-6612.	5.4	40
92	Backside power delivery as a scaling knob for future systems. , 2019, , .		7
93	Defect localization of metal interconnection lines in 3-dimensional through-silicon-via structures by differential scanning photocapacitance microscopy. Applied Physics Letters, 2018, 112, 071904.	1.5	4
94	Expected Failures in 3-D Technology and Related Failure Analysis Challenges. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2018, 8, 711-718.	1.4	18
95	RIE dynamics for extreme wafer thinning applications. Microelectronic Engineering, 2018, 192, 30-37.	1.1	15
96	Physics of self-aligned assembly at room temperature. Physics of Fluids, 2018, 30, .	1.6	2
97	Etch process modules development and integration in 3D-SOC applications. Microelectronic Engineering, 2018, 196, 38-48.	1.1	2
98	Anomalous ${C}$ â€“ ${V}$ Inversion in TSVs: The Problem and Its Cure. IEEE Transactions on Electron Devices, 2018, 65, 1473-1479.	1.6	2
99	An in-situ resistance measurement to extract IMC resistivity and kinetic parameter of alternative metallurgies for 3D stacking. , 2018, , .		2
100	Study of the influence of material properties and geometric parameters on warpage for Fan-Out Wafer Level Packaging. , 2018, , .		6
101	TCB optimization for stacking large thinned dies with 40 and 20 Î¼m pitch microbumps. , 2018, , .		4
102	Influence of Composition of SiCN Film for Surface Activated Bonding. ECS Transactions, 2018, 86, 159-168.	0.3	1
103	A Highly Reliable 1Ã—5Î¼m Via-last TSV Module. , 2018, , .		2
104	A study on substrate noise coupling among TSVs in 3D chip stack. IEICE Electronics Express, 2018, 15, 20180460-20180460.	0.3	3
105	Thermal Performance Comparison of Advanced 3D Packaging Concepts for Logic and Memory Integration in Mobile Cooling Conditions. , 2018, , .		3
106	Edge Trimming Induced Defects on Direct Bonded Wafers. Journal of Electronic Packaging, Transactions of the ASME, 2018, 140, .	1.2	6
107	Enhanced Cu pillar design to reduce thermomechanical stress induced during flip chip assembly. Microelectronics Reliability, 2018, 87, 97-105.	0.9	1
108	TSV process-induced MOS reliability degradation. , 2018, , .		5

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109	Extreme Thinned-Wafer Bonding Using Low Temperature Curable Polyimide for Advanced Wafer Level Integrations. , 2018, , .		3
110	Novel Failure Analysis Techniques for 1.8 Âµm Pitch Wafer-to-Wafer Bonding. , 2018, , .		1
111	A Novel Fan-Out Concept for Ultra-High Chip-to-Chip Interconnect Density with 20-Âµm Pitch. , 2018, , .		27
112	Advances in Temporary Bonding and Release Technology for Ultrathin Substrate Processing and High-Density Fan-Out Device Build-up. , 2018, , .		5
113	Characterization of Optical End-Point Detection for Via Reveal Processing. , 2018, , .		0
114	Impact of 1Î¼ m TSV via-last integration on electrical performance of advanced FinFET devices. , 2018, , .		9
115	"Hole-in-One TSV", a New Via Last Concept for High Density 3D-SOC Interconnects. , 2018, , .		10
116	Extreme Thinning of Si Wafers for Via-Last and Multi-wafer Stacking Applications. , 2018, , .		6
117	Improved Staggered Through Silicon Via Inductors for RF and Power Applications. , 2018, , .		2
118	Evaluation of Mechanical Stress Induced During IC Packaging. , 2018, , .		13
119	NOZZLE ARRAY SCALING EFFECTS ON THE THERMAL/HYDRAULIC PERFORMANCE OF LIQUID JET IMPINGEMENT COOLERS FOR HIGH PERFORMANCE ELECTRONIC APPLICATIONS. , 2018, , .		2
120	Edge trimming for surface activated dielectric bonded wafers. Microelectronic Engineering, 2017, 167, 10-16.	1.1	12
121	Characterization and Benchmarking of the Low Intertier Thermal Resistance of Three-Dimensional Hybrid Cu/Dielectric Wafer-to-Wafer Bonding. Journal of Electronic Packaging, Transactions of the ASME, 2017, 139, .	1.2	10
122	Convolution-Based Fast Thermal Model for 3-D-ICs: Transient Experimental Validation. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2017, , 1-16.	1.4	1
123	Alternative Cu pillar bumps design to reduce thermomechanical stress induced during flip chip assembly. , 2017, , .		0
124	Impact of backside process on high aspect ratio via-middle Cu through silicon via reliability. , 2017, , .		2
125	Influence of Si wafer thinning processes on (sub)surface defects. Applied Surface Science, 2017, 404, 82-87.	3.1	22
126	Growth rate of IMC in the binary sytems of Co/Sn and Cu/Sn. , 2017, , .		4

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127	Impact of via density and passivation thickness on the mechanical integrity of advanced Back-End-Of-Line interconnects. Microelectronics Reliability, 2017, 79, 297-305.	0.9	1
128	Advances in Thin Wafer Debonding and Ultrathin 28-nm FinFET Substrate Transfer. , 2017, , .		6
129	A Simple and Efficient RF Technique for TSV Characterization. , 2017, , .		1
130	Characterization of inorganic dielectric layers for low thermal budget wafer-to-wafer bonding. , 2017, , .		4
131	Lock-in thermal laser stimulation for non-destructive failure localization in 3-D devices. Microelectronics Reliability, 2017, 76-77, 188-193.	0.9	3
132	3D stacking cobalt and nickel microbumps and kinetics of corresponding IMCs at low temperatures. , 2017, , .		0
133	Scalable, sub 2Î¼m pitch, Cu/SiCN to Cu/SiCN hybrid wafer-to-wafer bonding technology. , 2017, , .		57
134	Interface charge trapping induced flatband voltage shift during plasma-enhanced atomic layer deposition in through silicon via. Journal of Applied Physics, 2017, 122, .	1.1	2
135	Investigation of Co Thin Film as Buffer Layer Applied to Cu/Sn Eutectic Bonding and UBM With Sn, SnCu, and SAC Solders Joints. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2017, 7, 1899-1905.	1.4	3
136	Statistical Distribution of Through-Silicon via Cu Pumping. IEEE Transactions on Device and Materials Reliability, 2017, 17, 549-559.	1.5	13
137	Assembly Technology for Fine Pitch Bumps Using Photodefinable Wafer-Level Underfill. Journal of Smart Processing, 2017, 6, 149-155.	0.0	0
138	A Unique Temporary Bond Solution Based on a Polymeric Material Tacky at Room Temperature and Highly Thermally Resistant Application Extension from 3D-SIC to FO-WLP. , 2017, , .		3
139	A novel in-situ resistance measurement to extract IMC resistivity and kinetic parameter for CoSn 3D stacks. , 2017, , .		2
140	Thermal Compression Bonding: Understanding Heat Transfer by in Situ Measurements and Modeling. , 2017, , .		11
141	High efficiency direct liquid jet impingement cooling of high power devices using a 3D-shaped polymer cooler. , 2017, , .		12
142	The Increasing Role of Polymers in Advanced Packaging - From Stress Buffer Layers to Wafer Level Underfills and Beyond. Journal of Photopolymer Science and Technology = [Fotoporima Konwakai Shi], 2017, 30, 17-24.	0.1	5
143	Packaging Material Evaluation for 2.5D/3D TSV Application. Transactions of the Japan Institute of Electronics Packaging, 2016, 9, E16-011-1-E16-011-7.	0.3	2
144	Continuity and reliability assessment of a scalable 3Ã—50Î¼m and 2Ã—40Î¼m via-middle TSV module. , 2016, , .		1

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145	Impact of ELD layers in mechanical properties of microbumps for 3D stacking. , 2016, , .		1
146	Small Pitch, High Aspect Ratio Via-Last TSV Module. , 2016, , .		19
147	Investigation of TSV noise coupling in 3D-ICs using an experimental validated 3D TSV circuit model including Si substrate effects and TSV capacitance inversion behavior after wafer thinning. , 2016, , .		2
148	Experimental Characterization of the Vertical and Lateral Heat Transfer in Three-Dimensional Stacked Die Packages. Journal of Electronic Packaging, Transactions of the ASME, 2016, 138, .	1.2	22
149	3D-SoC integration utilizing high accuracy wafer level bonding. , 2016, , .		3
150	3D IC assembly using thermal compression bonding and wafer-level underfill â€" Strategies for quality improvement and throughput enhancement. , 2016, , .		8
151	Characterization of Extreme Si Thinning Process for Wafer-to-Wafer Stacking. , 2016, , .		13
152	Fast and Accurate Modelling of Large TSV Arrays in 3D-ICs Using a 3D Circuit Model Validated Against Full-Wave FEM Simulations and RF Measurements. , 2016, , .		4
153	Technology optimization for high bandwidth density applications on 3D interposer. , 2016, , .		4
154	Liquid mediated direct bonding and bond propagation. , 2016, , .		1
155	Ultra-Fine Pitch 3D Integration Using Face-to-Face Hybrid Wafer Bonding Combined with a Via-Middle Through-Silicon-Via Process. , 2016, , .		38
156	Impact of wafer thinning on front-end reliability for 3D integration. , 2016, , .		5
157	Cost Comparison of Different TSV Implementation Options. , 2016, , .		0
158	Thermal characterization of the inter-die thermal resistance of hybrid Cu/dielectric wafer-to-wafer bonding. , 2016, , .		7
159	On the feasibility of die-to-wafer inorganic dielectric bonding. , 2016, , .		3
160	Development of multi-stack dielectric wafer bonding. , 2016, , .		6
161	Extremely Low-Force Debonding of Thinned CMOS Substrate by Laser Release of a Temporary Bonding Material. , 2016, , .		15
162	Fine Pitch Rapid Heat Self-Aligned Assembly and Liquid-Mediated Direct Bonding of Si Chips. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2016, 6, 946-953.	1.4	4

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163	The 3-D Interconnect Technology Landscape. IEEE Design and Test, 2016, 33, 8-20.	1.1	129
164	3D Stacking Using Bump-Less Process for Sub 10um Pitch Interconnects. , 2016, , .		18
165	Performance and Reliability Impact of Copper Plasticity in Backside TSV-Last Fabrication Process. IEEE Transactions on Device and Materials Reliability, 2016, 16, 402-412.	1.5	5
166	Low Warpage Wafer Level Transfer Molding Post 3D Die to Wafer Assembly. , 2016, , .		2
167	Surface Treatment to Enable Low Temperature and Pressure Copper Direct Bonding. , 2016, , .		3
168	Investigation of Advanced Dicing Technologies for Ultra Low-k and 3D Integration. , 2016, , .		9
169	Importance of alignment control during permanent bonding and its impact on via-last alignment for high density 3D interconnects. , 2016, , .		7
170	Die to wafer 3D stacking for below 10um pitch microbumps. , 2016, , .		6
171	Extreme wafer thinning optimization for via-last applications. , 2016, , .		11
172	High-density and low-leakage novel embedded 3D MIM capacitor on Si interposer. , 2016, , .		3
173	Impact of Via Density on the Mechanical Integrity of Advanced Back-End-of-Line During Packaging. , 2016, , .		9
174	3D stacking of Co- and Ni-based microbumps. , 2016, , .		12
175	Methodologies to mitigate package induced stresses in the BEOL. , 2016, , .		5
176	Dielectric liner reliability in via-middle through silicon vias with 3 Micron diameter. Microelectronic Engineering, 2016, 156, 37-40.	1.1	9
177	Reliable Via-Middle Copper Through-Silicon Via Technology for 3-D Integration. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2016, 6, 983-992.	1.4	13
178	Reliability Challenges Related to TSV Integration and 3-D Stacking. IEEE Design and Test, 2016, 33, 37-45.	1.1	29
179	Fast Transient Convolution-Based Thermal Modeling Methodology for Including the Package Thermal Impact in 3D ICs. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2016, 6, 424-431.	1.4	10
180	Packaging and Assembly Challenges for 2.5D/3D Devices. Additional Conferences (Device Packaging) Tj ETQq0 0 0 rgBT /Overlock 10 Tf	0.2	1

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181	Cobalt UBM for fine pitch microbump applications in 3DIC. , 2015, , .		9
182	Material technology for 2.5D/3D package. , 2015, , .		4
183	Development and Evaluation of Photodefinable Wafer Level Underfill. Journal of Photopolymer Science and Technology = [Fotoporima Konwakai Shi], 2015, 28, 229-232.	0.1	3
184	An Efficient Bump Pad Design to Mitigate the Flip Chip Package Induced Stress. , 2015, , .		3
185	Enabling pre-assembly process of 3D wafers with high topography at the backside. , 2015, , .		0
186	Comparison of properties of thermo-compression bonded 3D stacks using a liquid and a dry-film wafer level underfills. , 2015, , .		0
187	Through silicon via to FinFET noise coupling in 3-D integrated circuits. , 2015, , .		2
188	Impact of backside processing on C-V characteristics of TSV capacitors in 3D stacked IC process flows. , 2015, , .		3
189	Thermal compression bonding of 20 Î¼m pitch micro bumps with pre-applied underfill - Process and reliability. , 2015, , .		5
190	An alternative 3D packaging route through wafer reconstruction. , 2015, , .		0
191	Effect of test structure on electromigration characteristics in three-dimensional through silicon via stacked devices. Japanese Journal of Applied Physics, 2015, 54, 05EE01.	0.8	16
192	Permanent wafer bonding in the low temperature by using various plasma enhanced chemical vapour deposition dielectrics. , 2015, , .		23
193	Reliability study of liner/barrier/seed options for via-middle TSV's with 3 micron diameter and below. , 2015, , .		2
194	ESD protection design in active-lite interposer for 2.5 and 3D systems-in-package. , 2015, , .		5
195	3D-convolution based fast transient thermal model for 3D integrated circuits: methodology and applications. , 2015, , .		6
196	Microstructure simulation of grain growth in Cu through silicon vias using phase-field modeling. Microelectronics Reliability, 2015, 55, 765-770.	0.9	13
197	Modeling the effect of charges in the back side passivation layer on through silicon via (TSV) capacitance after wafer thinning. , 2015, , .		5
198	Experimental Characterization of the Vertical and Lateral Heat Transfer in 3D-SIC Packages. , 2015, , .		8

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199	Analysis of copper plasticity impact in TSV-middle and backside TSV-last fabrication processes. , 2015, , .		4
200	Formation, processing and characterization of Coâ€“Sn intermetallic compounds for potential integration in 3D interconnects. Microelectronic Engineering, 2015, 140, 72-80.	1.1	39
201	A novel structure of MOSFET array to measure ioff-ion with high accuracy and high density. , 2015, , .		2
202	Demonstration of a novel low cost single material temporary bond solution for high topography substrates based on a mechanical wafer debonding and innovative adhesive removal. , 2015, , .		5
203	Noise coupling between TSVs and active devices: Planar nMOSFETs vs. nFinFETs. , 2015, , .		6
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