Eric Beyne

List of Publications by Year
in descending order

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472	6,164	159525 30	189801 50
papers	citations	h-index	g-index

479	479	479	2359
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Design Issues and Considerations for Low-Cost 3-D TSV IC Technology. IEEE Journal of Solid-State Circuits, 2011, 46, 293-307.	3.5	236
2	MEMS for wireless communications: Âfrom RF-MEMS components to RF-MEMS-SiPÂ. Journal of Micromechanics and Microengineering, 2003, 13, S139-S163.	1.5	200
3	The 3-D Interconnect Technology Landscape. IEEE Design and Test, 2016, 33, 8-20.	1.1	129
4	Cu pumping in TSVs: Effect of pre-CMP thermal budget. Microelectronics Reliability, 2011, 51, 1856-1859.	0.9	122
5	3D stacked IC demonstration using a through Silicon Via First approach. , 2008, , .		113
6	Thermal cycling reliability of SnAgCu and SnPb solder joints: A comparison for several IC-packages. Microelectronics Reliability, 2007, 47, 259-265.	0.9	103
7	Multilayer thin-film MCM-D for the integration of high-performance RF and microwave circuits. IEEE Transactions on Components and Packaging Technologies, 2001, 24, 510-519.	1.4	96
8	Bow-tie slot antenna fed by CPW. Electronics Letters, 1999, 35, 514.	0.5	94
9	Wafer-Level Packaging Technology for High-<tex>Q</tex>On-Chip Inductors and Transmission Lines. IEEE Transactions on Microwave Theory and Techniques, 2004, 52, 1244-1251.	2.9	80
10	The indent reflow sealing (IRS) technique-a method for the fabrication of sealed cavities for MEMS devices. Journal of Microelectromechanical Systems, 2000, 9, 206-217.	1.7	76
11	Electrodeposition for the synthesis of microsystems. Journal of Micromechanics and Microengineering, 2000, 10, 101-107.	1.5	76
12	3D System Integration Technologies. International Power Modulator Symposium and High-Voltage Workshop, 2006, , .	0.0	76
13	Impact of 3D design choices on manufacturing cost. , 2009, , .		73
14	Impact of the electrodeposition chemistry used for TSV filling on the microstructural and thermo-mechanical response of Cu. Journal of Materials Science, 2011, 46, 3868-3882.	1.7	69
15	Integration challenges of copper Through Silicon Via (TSV) metallization for 3D-stacked IC integration. Microelectronic Engineering, 2011, 88, 745-748.	1.1	66
16	Accurate modeling of high-Q spiral inductors in thin-film multilayer technology for wireless telecommunication applications. IEEE Transactions on Microwave Theory and Techniques, 2001, 49, 589-599.	2.9	64
17	Through-silicon via and die stacking technologies for microsystems-integration. , 2008, , .		64
18	A generic methodology for deriving compact dynamic thermal models, applied to the PSGA package. IEEE Transactions on Components and Packaging Technologies, 1998, 21, 565-576.	0.7	60

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19	Chip-package codesign of a low-power 5-GHz RF front end. Proceedings of the IEEE, 2000, 88, 1583-1597.	16.4	58
20	3D stacked ICs using Cu TSVs and Die to Wafer Hybrid Collective bonding. , 2009, , .		58
21	Scalable, sub 2Î¼m pitch, Cu/SiCN to Cu/SiCN hybrid wafer-to-wafer bonding technology. , 2017, , .		57
22	Degradation of Cu6Sn5 intermetallic compound by pore formation in solidâ€"liquid interdiffusion Cu/Sn microbump interconnects. Microelectronic Engineering, 2014, 117, 26-34.	1.1	56
23	3D System Integration Technologies. , 2007, , .		55
24	3-D Technology Assessment: Path-Finding the Technology/Design Sweet-Spot. Proceedings of the IEEE, 2009, 97, 96-107.	16.4	47
25	Design issues and considerations for low-cost 3D TSV IC technology. , 2010, , .		47
26	3-D Wafer-Level Packaging Die Stacking Using Spin-on-Dielectric Polymer Liner Through-Silicon Vias. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2011, 1, 833-840.	1.4	47
27	Impact of post-plating anneal and through-silicon via dimensions on Cu pumping. , 2013, , .		46
28	Mechanical FEM Simulation of Bonding Process on Cu Lowk Wafers. IEEE Transactions on Components and Packaging Technologies, 2004, 27, 643-650.	1.4	44
29	Thermal modeling and management in ultrathin chip stack technology. IEEE Transactions on Components and Packaging Technologies, 2002, 25, 244-253.	1.4	43
30	Technologies for highly miniaturized autonomous sensor networks. Microelectronics Journal, 2006, 37, 1563-1568.	1.1	43
31	Simultaneous Cu-Cu and Compliant Dielectric Bonding for 3D Stacking of ICs. , 2007, , .		43
32	CPW-fed cusp antenna. Microwave and Optical Technology Letters, 1999, 22, 288-290.	0.9	42
33	SOP Integration and Codesign of Antennas. IEEE Transactions on Advanced Packaging, 2004, 27, 341-351.	1.7	42
34	Novel Cu/SiCN surface topography control for 1 Î¼m pitch hybrid wafer-to-wafer bonding. , 2020, , .		41
35	Analysis of the Induced Stresses in Silicon During Thermcompression Cu-Cu Bonding of Cu-Through-Vias in 3D-SIC Architecture. , 2007, , .		40
36	Integration of TSVs, wafer thinning and backside passivation on full 300mm CMOS wafers for 3D applications. , 2011, , .		40

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37	High-Efficiency Polymer-Based Direct Multi-Jet Impingement Cooling Solution for High-Power Devices. IEEE Transactions on Power Electronics, 2019, 34, 6601-6612.	5.4	40
38	Direct gold and copper wires bonding on copper. Microelectronics Reliability, 2003, 43, 913-923.	0.9	39
39	Correlation between Cu microstructure and TSV Cu pumping. , 2014, , .		39
40	Formation, processing and characterization of Coâ€“Sn intermetallic compounds for potential integration in 3D interconnects. Microelectronic Engineering, 2015, 140, 72-80.	1.1	39
41	Ultra-Fine Pitch 3D Integration Using Face-to-Face Hybrid Wafer Bonding Combined with a Via-Middle Through-Silicon-Via Process. , 2016, , .		38
42	Elimination Of The Axial Deformation Problem Of Cu-TSV In 3D Integration. AIP Conference Proceedings, 2010, , .	0.3	37
43	Parameterized Modeling of Thermomechanical Reliability for CSP Assemblies. Journal of Electronic Packaging, Transactions of the ASME, 2003, 125, 498-505.	1.2	35
44	Thermo-mechanics of 3D-wafer level and 3D stacked IC packaging technologies. , 2008, , .		35
45	Void-Free Filling of HAR TSVs Using a Wet Alkaline Cu Seed on CVD Co as a Replacement for PVD Cu Seed. Journal of the Electrochemical Society, 2011, 158, H160.	1.3	35
46	Resistance to electromigration of purely intermetallic micro-bump interconnections for 3D-device stacking. , 2008, , .		32
47	Solving Technical and Economical Barriers to the Adoption of Through-Si-Via 3D Integration Technologies. , 2008, , .		32
48	Influence of Composition of SiCN as Interfacial Layer on Plasma Activated Direct Bonding. ECS Journal of Solid State Science and Technology, 2019, 8, P346-P350.	0.9	31
49	Experimental characterization and model validation of liquid jet impingement cooling using a high spatial resolution and programmable thermal test chip. Applied Thermal Engineering, 2019, 152, 308-318.	3.0	31
50	In-depth Raman spectroscopy analysis of various parameters affecting the mechanical stress near the surface and bulk of Cu-TSVs. , 2012, , .		30
51	Reliability Challenges Related to TSV Integration and 3-D Stacking. IEEE Design and Test, 2016, 33, 37-45.	1.1	29
52	Inductance and quality-factor evaluation of planar lumped inductors in a multilayer configuration. IEEE Transactions on Microwave Theory and Techniques, 1997, 45, 918-923.	2.9	28
53	Thermomechanical models for leadless solder interconnections in flip chip assemblies. IEEE Transactions on Components and Packaging Technologies, 1998, 21, 177-185.	0.7	28
54	High-Q Above-IC Inductors Using Thin-Film Wafer-Level Packaging Technology Demonstrated on 90-nm RF-CMOS 5-GHz VCO and 24-GHz LNA. IEEE Transactions on Advanced Packaging, 2006, 29, 810-817.	1.7	28

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55	Polymer Filling of Silicon Trenches for 3-D Through Silicon vias Applications. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2011, 1, 825-832.	1.4	28
56	Impact of through silicon via induced mechanical stress on fully depleted Bulk FinFET technology. , 2012, , .		28
57	Electrically yielding Collective Hybrid Bonding for 3D stacking of ICs. , 2009, , .		27
58	Ultrathin wafer handling in 3D Stacked IC manufacturing combining a novel ZoneBOND™ temporary bonding process with room temperature peel debonding. , 2012, , .		27
59	A Novel Fan-Out Concept for Ultra-High Chip-to-Chip Interconnect Density with 20-Âµm Pitch. , 2018, , .		27
60	3D stacking induced mechanical stress effects. , 2014, , .		26
61	Extreme Wafer Thinning and nano-TSV processing for 3D Heterogeneous Integration. , 2020, , .		26
62	Die stacking using 3D-wafer level packaging copper/polymer through-si via technology and Cu/Sn interconnect bumping. , 2009, , .		25
63	Cost effectiveness of 3D integration options. , 2010, , .		25
64	Experimental and numerical investigation of direct liquid jet impinging cooling using 3D printed manifolds on lidded and lidless packages for 2.5D integrated systems. Applied Thermal Engineering, 2020, 164, 114535.	3.0	24
65	Compact thermal modeling of hot spots in advanced 3D-stacked ICs. , 2009, , .		23
66	Enhanced barrier seed metallization for integration of high-density high aspect-ratio copper-filled 3D through-silicon via interconnects. , 2012, , .		23
67	Permanent wafer bonding in the low temperature by using various plasma enhanced chemical vapour deposition dielectrics. , 2015, , .		23
68	Integrated high-frequency inductors using amorphous electrodeposited Co-P core. IEEE Transactions on Magnetics, 2002, 38, 3498-3500.	1.2	22
69	Experimental Characterization of the Vertical and Lateral Heat Transfer in Three-Dimensional Stacked Die Packages. Journal of Electronic Packaging, Transactions of the ASME, 2016, 138, .	1.2	22
70	Influence of Si wafer thinning processes on (sub)surface defects. Applied Surface Science, 2017, 404, 82-87.	3.1	22
71	Electrical, thermal and mechanical impact of 3D TSV and 3D stacking technology on advanced CMOS devices — Technology directions. , 2012, , .		21
72	Integration and manufacturing aspects of moving from WaferBOND HT-10.10 to ZoneBOND material in temporary wafer bonding and debonding for 3D applications. , 2013, , .		21

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73	Development of underfilling and thermo-compression bonding processes for stacking multi-layer 3D ICs. , 2014, , .		21
74	Enabling Ultra-Thin Die to Wafer Hybrid Bonding for Future Heterogeneous Integrated Systems. , 2019, , .		21
75	Low-Cost Energy-Efficient On-Chip Hotspot Targeted Microjet Cooling for High- Power Electronics. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 577-589.	1.4	21
76	Power Delivery Network (PDN) Modeling for Backside-PDN Configurations With Buried Power Rails and mu TSVs. IEEE Transactions on Electron Devices, 2020, 67, 11-17.	1.6	21
77	Characterization of through-silicon vias using laser terahertz emission microscopy. Nature Electronics, 2021, 4, 202-207.	13.1	21
78	Modified microâ€“macro thermo-mechanical modelling of ceramic ball grid array packages. Microelectronics Reliability, 2003, 43, 307-318.	0.9	20
79	Interposer technology for high band width interconnect applications. , 2013, , .		20
80	3D SoC integration, beyond 2.5D chiplets. , 2021, , .		20
81	Numerically efficient spatial-domain moment method for multislot transmission lines in layered media-application to multislot lines in MCM-D technology. IEEE Transactions on Microwave Theory and Techniques, 1999, 47, 1782-1787.	2.9	19
82	Numerical and experimental characterization of the thermal behavior of a packaged DRAM-on-logic stack. , 2012, , .		19
83	Copper through silicon via induced keep out zone for 10nm node bulk FinFET CMOS technology. , 2013, , .		19
84	Measurements and Analysis of Substrate Noise Coupling in TSV-Based 3-D Integrated Circuits. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2014, 4, 1026-1037.	1.4	19
85	Small Pitch, High Aspect Ratio Via-Last TSV Module. , 2016, , .		19
86	Accelerated ageing with <i>in situ</i> electrical testing: A powerful tool for the buildingâ€in approach to quality and reliability in electronics. Quality and Reliability Engineering International, 1994, 10, 15-26.	1.4	18
87	Circularly polarised aperture antenna fed by CPW and built in the MCM-D technology. Electronics Letters, 1999, 35, 250.	0.5	18
88	Improved thermal fatigue reliability for flip chip assemblies using redistribution techniques. IEEE Transactions on Advanced Packaging, 2000, 23, 239-246.	1.7	18
89	Prediction of the Influence of Induced Stresses in Silicon on CMOS Performance in a Cu-Through-Via Interconnect Technology. , 2007, , .		18
90	Parylene N as a dielectric material for through silicon vias. , 2008, , .		18

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91	Insertion bonding: A novel Cu-Cu bonding approach for 3D integration. , 2010, , .		18
92	Ni/Cu/Sn bumping scheme for fine-pitch micro-bump connections. , 2011, , .		18
93	Steady state and transient thermal analysis of hot spots in 3D stacked ICs using dedicated test chips. , 2011, , .		18
94	Chip package interaction (CPI): Thermo mechanical challenges in 3D technologies. , 2012, , .		18
95	3D Stacking Using Bump-Less Process for Sub 10um Pitch Interconnects. , 2016, , .		18
96	Expected Failures in 3-D Technology and Related Failure Analysis Challenges. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2018, 8, 711-718.	1.4	18
97	Entire Domain Basis Function Expansion of the Differential Surface Admittance for Efficient Broadband Characterization of Lossy Interconnects. IEEE Transactions on Microwave Theory and Techniques, 2020, 68, 1217-1233.	2.9	18
98	Impact of through silicon vias on front-end-of-line performance after thermal cycling and thermal storage. , 2012, , .		17
99	Full-wave analysis of multiconductor multislot planar guiding structures in layered media. IEEE Transactions on Microwave Theory and Techniques, 2003, 51, 874-886.	2.9	16
100	Ultra low stress and low temperature patternable silicone materials for applications within microelectronics. Microelectronic Engineering, 2004, 76, 212-218.	1.1	16
101	Chip-Package Interaction in 3D stacked IC packages using Finite Element Modelling. Microelectronics Reliability, 2014, 54, 1200-1205.	0.9	16
102	Effect of test structure on electromigration characteristics in three-dimensional through silicon via stacked devices. Japanese Journal of Applied Physics, 2015, 54, 05EE01.	0.8	16
103	Suppression of the parasitic modes in CPW discontinuities using MCM-D technology-application to a novel 3-dB power splitter. IEEE Transactions on Microwave Theory and Techniques, 1998, 46, 2426-2430.	2.9	15
104	X-band brick wall antenna fed by CPW. Electronics Letters, 1998, 34, 836.	0.5	15
105	Generalized analysis of coupled lines in multilayer microwave MCM-D technology-application: integrated coplanar Lange couplers. IEEE Transactions on Microwave Theory and Techniques, 1999, 47, 1863-1872.	2.9	15
106	3D Embedding and Interconnection of Ultra Thin (≪ 20 μm) Silicon Dies. , 2007, , .		15
107	Technology Assessment of Through-Silicon Via by Using Câ€“V and Câ€“t Measurements. IEEE Electron Device Letters, 2011, 32, 946-948.	2.2	15
108	Characterization of the thermal impact of Cu-Cu bonds achieved using TSVs on hot spot dissipation in 3D stacked ICs. , 2011, , .		15

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109	FET arrays as CPI sensors for 3D stacking and packaging characterization. , 2012, , .		15
110	Extremely Low-Force Debonding of Thinned CMOS Substrate by Laser Release of a Temporary Bonding Material. , 2016, , .		15
111	RIE dynamics for extreme wafer thinning applications. Microelectronic Engineering, 2018, 192, 30-37.	1.1	15
112	Antenna arrays in MCM-D technology fed by coplanar CPW networks. IEEE Transactions on Microwave Theory and Techniques, 2000, 48, 1065-1068.	2.9	14
113	300mm wafer thinning and backside passivation compatibility with temporary wafer bonding for 3D stacked IC applications. , 2010, , .		14
114	High frequency scanning acoustic microscopy applied to 3D integrated process: Void detection in Through Silicon Vias. , 2013, , .		14
115	Reflow process optimization for micro-bumps applications in 3D technology. , 2014, , .		14
116	Minimizing interposer warpage by process control and design optimization. , 2014, , .		14
117	Conjugate Heat Transfer and Fluid Flow Modeling for Liquid Microjet Impingement Cooling with Alternating Feeding and Draining Channels. Fluids, 2019, 4, 145.	0.8	14
118	Wafer-level package interconnect options. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006, 14, 654-659.	2.1	13
119	Impact of thinning and through silicon via proximity on High-k / Metal Gate first CMOS performance. , 2010, , .		13
120	Fast convolution based thermal model for 3D-ICs: Methodology, accuracy analysis and package impact. Microelectronics Journal, 2014, 45, 1746-1752.	1.1	13
121	Microstructure simulation of grain growth in Cu through silicon vias using phase-field modeling. Microelectronics Reliability, 2015, 55, 765-770.	0.9	13
122	Impact of oxide liner properties on TSV Cu pumping and TSV stress. , 2015, , .		13
123	Characterization of Extreme Si Thinning Process for Wafer-to-Wafer Stacking. , 2016, , .		13
124	Reliable Via-Middle Copper Through-Silicon Via Technology for 3-D Integration. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2016, 6, 983-992.	1.4	13
125	Statistical Distribution of Through-Silicon via Cu Pumping. IEEE Transactions on Device and Materials Reliability, 2017, 17, 549-559.	1.5	13
126	Evaluation of Mechanical Stress Induced During IC Packaging. , 2018, , .		13

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127	Experimental Characterization of a Chip-Level 3-D Printed Microjet Liquid Impingement Cooler for High-Performance Systems. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019, 9, 1815-1824.	1.4	13
128	Characterization of bonding activation sequences to enable ultra-low Cu/SiCN wafer level hybrid bonding. , 2021, , .		13
129	Photopatternable silicone compositions for electronic packaging applications. , 2004, , .		12
130	Through-Silicon via Technology for 3D IC. , 2011, , 93-108.		12
131	Transient analysis based thermal characterization of die-die interfaces in 3D-ICs. , 2012, , .		12
132	Experimental thermal characterization and thermal model validation of 3D packages using a programmable thermal test chip. , 2015, , .		12
133	3D stacking of Co- and Ni-based microbumps. , 2016, , .		12
134	Edge trimming for surface activated dielectric bonded wafers. Microelectronic Engineering, 2017, 167, 10-16.	1.1	12
135	High efficiency direct liquid jet impingement cooling of high power devices using a 3D-shaped polymer cooler. , 2017, , .		12
136	Effects of isothermal storage on grain structure of Cu/Sn/Cu microbump interconnects for 3D stacking. Microelectronics Reliability, 2019, 102, 113296.	0.9	12
137	3D-SIP Integration for Autonomous Sensor Nodes. , 0, , .		11
138	Extreme wafer thinning optimization for via-last applications. , 2016, , .		11
139	Thermal Compression Bonding: Understanding Heat Transfer by in Situ Measurements and Modeling. , 2017, , .		11
140	Advanced Dicing Technologies for Combination of Wafer to Wafer and Collective Die to Wafer Direct Bonding. , 2019, , .		11
141	Study of the effect of Sn grain boundaries on IMC morphology in solid state inter-diffusion soldering. Scientific Reports, 2019, 9, 14862.	1.6	11
142	Direct Bonding of low Temperature Heterogeneous Dielectrics. , 2019, , .		11
143	Modeling Copper Plastic Deformation and Liner Viscoelastic Flow Effects on Performance and Reliability in Through Silicon Via (TSV) Fabrication Processes. IEEE Transactions on Device and Materials Reliability, 2019, 19, 642-653.	1.5	11
144	Nozzle scaling effects for the thermohydraulic performance of microjet impingement cooling with distributed returns. Applied Thermal Engineering, 2020, 180, 115767.	3.0	11

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145	Introduction of a New Carrier System for Collective Die-to-Wafer Hybrid Bonding and Laser-Assisted Die Transfer. , 2020, , .		11
146	10 and 7 Î¼m Pitch Thermo-compression Solder Joint, Using A Novel Solder Pillar And Metal Spacer Process. , 2020, , .		11
147	Reliability Study of Polymers Used in Sub-4-Î¼m Pitch RDL Applications. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2021, 11, 1073-1080.	1.4	11
148	Film Characterization of Low-Temperature Silicon Carbon Nitride for Direct Bonding Applications. ECS Journal of Solid State Science and Technology, 2020, 9, 123011.	0.9	11
149	Brick-wall antenna in multilayer thin-film technology. Microwave and Optical Technology Letters, 1998, 19, 360-365.	0.9	10
150	Electrical field induced ageing of polymer light-emitting diodes in an oxygen-rich atmosphere studied by emission microscopy, scanning electron microscopy and secondary ion mass spectroscopy. Synthetic Metals, 1998, 96, 87-96.	2.1	10
151	Spiral inductors integrated in MCM-D using the design space concept. , 0, , .		10
152	The influence of packaging materials on RF performance. Microelectronics Reliability, 2003, 43, 351-357.	0.9	10
153	Verifying electrical/thermal/thermo-mechanical behavior of a 3D stack - Challenges and solutions. , 2010, , .		10
154	3D technology roadmap and status. , 2011, , .		10
155	Metrology and inspection for process control during bonding and thinning of stacked wafers for manufacturing 3D SIC's. , 2011, , .		10
156	Highly-conformal plasma-enhanced atomic-layer deposition silicon dioxide liner for high aspect-ratio through-silicon via 3D interconnections. , 2012, , .		10
157	Comparative study of 3D stacked IC and 3D interposer integration: Processing and assembly challenges. , 2014, , .		10
158	Fast Transient Convolution-Based Thermal Modeling Methodology for Including the Package Thermal Impact in 3D ICs. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2016, 6, 424-431.	1.4	10
159	Characterization and Benchmarking of the Low Intertier Thermal Resistance of Three-Dimensional Hybrid Cu/Dielectric Wafer-to-Wafer Bonding. Journal of Electronic Packaging, Transactions of the ASME, 2017, 139, .	1.2	10
160	"Hole-in-One TSV", a New Via Last Concept for High Density 3D-SOC Interconnects. , 2018, , .		10
161	A Highly Reliable 1.4Î¼m Pitch Via-Last TSV Module for Wafer-to-Wafer Hybrid Bonded 3D-SOC Systems. , 2019, , .		10
162	Protective Layer for Collective Die to Wafer Hybrid Bonding. , 2019, , .		10

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163	Photosensitive polymer reliability for fine pitch RDL applications. , 2020, , .		10
164	Demonstration of a collective hybrid die-to-wafer integration. , 2020, , .		10
165	Advances in Photosensitive Polymer Based Damascene RDL Processes: Toward Submicrometer Pitches With More Metal Layers. , 2021, , .		10
166	3D Wafer Level Packaging Approach Towards Cost Effective Low Loss High Density 3D Stacking. , 2006, , .		9
167	Outperformance of Cu pillar flip chip bumps in electromigration testing. , 2011, , .		9
168	Effect of TSV presence on FEOL yield and reliability. , 2013, , .		9
169	Numerical comparison of the thermal performance of 3D stacking and Si interposer based packaging concepts. , 2013, , .		9
170	Hydrogen outgassing induced liner/barrier reliability degradation in through silicon via's. Applied Physics Letters, 2014, 104, 142906.	1.5	9
171	Impact of Cu TSVs on BEOL metal and dielectric reliability. , 2014, , .		9
172	W2W permanent stacking for 3D system integration. , 2014, , .		9
173	Reliability challenges for barrier/liner system in high aspect ratio through silicon vias. Microelectronics Reliability, 2014, 54, 1949-1952.	0.9	9
174	Cobalt UBM for fine pitch microbump applications in 3DIC. , 2015, , .		9
175	Advanced metallization scheme for 3Ã—50Âµm via middle TSV and beyond. , 2015, , .		9
176	Effects of packaging on mechanical stress in 3D-ICs. , 2015, , .		9
177	Investigation of Advanced Dicing Technologies for Ultra Low-k and 3D Integration. , 2016, , .		9
178	Impact of Via Density on the Mechanical Integrity of Advanced Back-End-of-Line During Packaging. , 2016, , .		9
179	Dielectric liner reliability in via-middle through silicon vias with 3 Micron diameter. Microelectronic Engineering, 2016, 156, 37-40.	1.1	9
180	Impact of 1Î¼m TSV via-last integration on electrical performance of advanced FinFET devices. , 2018, , .		9

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181	Advances in Temporary Carrier Technology for High-Density Fan-Out Device Build-up. , 2019, , .		9
182	3D Wafer-to-Wafer Bonding Thermal Resistance Comparison: Hybrid Cu/dielectric Bonding versus Dielectric via-last Bonding. , 2020, , .		9
183	Experimental and Numerical Study of 3-D Printed Direct Jet Impingement Cooling for High-Power, Large Die Size Applications. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2021, 11, 415-425.	1.4	9
184	Buried Power Rails and Nano-Scale TSV: Technology Boosters for Backside Power Delivery Network and 3D Heterogeneous Integration. , 2022, , .		9
185	A MCM-D-type module for the ATLAS pixel detector. IEEE Transactions on Nuclear Science, 1999, 46, 1861-1864.	1.2	8
186	Direct Au and Cu wire bonding on Cu/low-k BEOL. , 0, , .		8
187	Fine pitch copper wire bonding on copper bond pad process optimization. , 0, , .		8
188	Multilayer thin-film technology enabling technology for solving high-density interconnect and assembly problems. Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 2003, 509, 191-199.	0.7	8
189	Modeling and characterization of the polymer stud grid array (PSGA) package: electrical, thermal and thermo-mechanical qualification. IEEE Transactions on Electronics Packaging Manufacturing, 2003, 26, 54-67.	1.6	8
190	Sequential-rotation arrays of circularly polarized aperture antennas in the MCM-D technology. Microwave and Optical Technology Letters, 2005, 44, 581-585.	0.9	8
191	Technology platform for 3-D stacking of thinned embedded dies. , 2008, , .		8
192	Reliability concerns in copper TSV's: Methods and results. , 2012, , .		8
193	Process characterization of thin wafer debonding with thermoplastic materials. , 2012, , .		8
194	Simulation of Cu pumping during TSV fabrication. , 2013, , .		8
195	Via-middle through-silicon via with integrated airgap to zero TSV-induced stress impact on device performance. , 2013, , .		8
196	Experimental Characterization of the Vertical and Lateral Heat Transfer in 3D-SIC Packages. , 2015, , .		8
197	3D IC assembly using thermal compression bonding and wafer-level underfill â€" Strategies for quality improvement and throughput enhancement. , 2016, , .		8
198	Design Enablement of Fine Pitch Face-to-Face 3D System Integration using Die-by-Die Place & Route. , 2019, , .		8

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199	The Growing Application Field of Laser Debonding: From Advanced Packaging to Future Nanoelectronics. , 2019, , .		8
200	Morphological characterization and mechanical behavior by dicing and thinning on direct bonded Si wafer. Journal of Manufacturing Processes, 2020, 58, 811-818.	2.8	8
201	Optical Beam-Based Defect Localization Methodologies for Open and Short Failures in Micrometer-Scale 3-D TSV Interconnects. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 1542-1551.	1.4	8
202	Area-Selective Electroless Deposition of Cu for Hybrid Bonding. IEEE Electron Device Letters, 2021, 42, 1826-1829.	2.2	8
203	Direct Bonding Using Low Temperature SiCN Dielectrics. , 2022, , .		8
204	Broadband modeling and transient analysis of MCM interconnections. IEEE Transactions on Advanced Packaging, 1994, 17, 153-160.	0.7	7
205	Performance analysis of MCM systems. IEEE Transactions on Advanced Packaging, 1997, 20, 334-341.	0.7	7
206	Advances in microwave MCMâ€Ð technology. Microelectronics International, 2000, 17, 19-22.	0.4	7
207	Chip-package co-design of a 4.7 GHz VCO. , 2000, , .		7
208	Characterisation, Modelling and Design of Bond-Wire Interconnects for Chip-Package Co-Design. , 2003, , .		7
209	Cu interconnects and low-k dielectrics, challenges for chip interconnections and packaging. , 0, , .		7
210	Optimizing Au and In micro-bumping for 3D chip stacking. , 2008, , .		7
211	Zero-level packaging for (RF-)MEMS implementing TSVs and metal bonding. , 2011, , .		7
212	Novel Cuâ€"Cu Bonding Technique: The Insertion Bonding Approach. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2011, 1, 1885-1894.	1.4	7
213	Thermal stability of copper Through-Silicon Via barriers during IC processing. , 2011, , .		7
214	On the thermal stability of physically-vapor-deposited diffusion barriers in 3D Through-Silicon Vias during IC processing. Microelectronic Engineering, 2013, 106, 155-159.	1.1	7
215	Design issues in heterogeneous 3D/2.5D integration. , 2013, , .		7
216	System Level Comparison of 3D Integration Technologies for Future Mobile MPSoC Platform. IEEE Embedded Systems Letters, 2014, 6, 85-88.	1.3	7

#	Article	IF	Citations
217	Defect detection in Through Silicon Vias by GHz Scanning Acoustic Microscopy: Key ultrasonic characteristics. , 2014, , .		7
218	Thermal characterization of the inter-die thermal resistance of hybrid Cu/dielectric wafer-to-wafer bonding. , 2016, , .		7
219	Importance of alignment control during permanent bonding and its impact on via-last alignment for high density 3D interconnects. , 2016, , .		7
220	In-Line Metrology for Characterization and Control of Extreme Wafer Thinning of Bonded Wafers. IEEE Transactions on Semiconductor Manufacturing, 2019, 32, 54-61.	1.4	7
221	Fine-pitch bonding technology with surface-planarized solder micro-bump/polymer hybrid for 3D integration. Japanese Journal of Applied Physics, 2021, 60, 026502.	0.8	7
222	Acoustic modulation during laser debonding of collective hybrid bonded dies. , 2021, , .		7
223	Heat transfer and pressure drop correlations for direct on-chip microscale jet impingement cooling with alternating feeding and draining jets. International Journal of Heat and Mass Transfer, 2022, 182, 121865.	2.5	7
224	Backside power delivery as a scaling knob for future systems. , 2019, , .		7
225	A new method of synthesizing high-Tc superconducting materials. Physica C: Superconductivity and Its Applications, 1989, 162-164, 881-882.	0.6	6
226	CIMID, a technology for high density integration of electronic systems. , 0, , .		6
227	2 Ã— 2 and 4 Ã— 4 arrays of annular slot antennas in MCM-D technology fed by coplanar CPW networks. IET Microwaves Antennas and Propagation, 1999, 146, 335.	1.2	6
228	MCM-D technology for integrated passives components. , 2000, , .		6
229	High density interconnect substrates using multilayer thin film technology on laminate substrates (MCMâ€SL/D). Microelectronics International, 2001, 18, 36-42.	0.4	6
230	Parametric compact models for the 72-pins polymer stud grid arrayâ„¢. Microelectronics Journal, 2001, 32, 839-846.	1.1	6
231	Introducing a silicone under the bump configuration for stress relief in a wafer level package. , 0, , .		6
232	Characterization and FE analysis on the shear test of electronic materials. Microelectronics Reliability, 2004, 44, 1915-1921.	0.9	6
233	Multimodal Characterization of Planar Microwave Structures. IEEE Transactions on Microwave Theory and Techniques, 2004, 52, 175-182.	2.9	6
234	Low Temperature Technology Options for Integrated High Density Capacitors. , 0, , .		6

#	Article	IF	Citations
235	Electrical characterization, modeling and reliability analysis of a via last TSV. , 2010, , .		6
236	Cost comparison between 3D and 2.5D integration. , 2012, , .		6
237	Comparison of x-ray diffraction, wafer curvature and Raman spectroscopy to evaluate the stress evolution in Copper TSV's. , 2012, , .		6
238	Wafer applied and no flow underfill screening for 3D stacks. , 2012, , .		6
239	Convolution based compact thermal model for 3D-ICs: Methodology and accuracy analysis. , 2013, , .		6
240	Wafer reconstruction: An alternative 3D integration process flow. , 2013, , .		6
241	Si interposer build-up options and impact on 3D system cost. , 2013, , .		6
242	Impact of 3D integration on 7nm high mobility channel devices operating in the ballistic regime. , 2014, , .		6
243	Large area interposer lithography. , 2014, , .		6
244	The underfill-microbump interaction mechanism in 3D ICs: Impact and mitigation of induced stresses. , 2014, , .		6
245	3D-convolution based fast transient thermal model for 3D integrated circuits: methodology and applications. , 2015, , .		6
246	Noise coupling between TSVs and active devices: Planar nMOSFETs vs. nFinFETs. , 2015, , .		6
247	Single-release-layer process for temporary bonding applications in the 3D integration area. , 2015, , .		6
248	Development of multi-stack dielectric wafer bonding. , 2016, , .		6
249	Die to wafer 3D stacking for below 10um pitch microbumps. , 2016, , .		6
250	Advances in Thin Wafer Debonding and Ultrathin 28-nm FinFET Substrate Transfer. , 2017, , .		6
251	Study of the influence of material properties and geometric parameters on warpage for Fan-Out Wafer Level Packaging. , 2018, , .		6
252	Edge Trimming Induced Defects on Direct Bonded Wafers. Journal of Electronic Packaging, Transactions of the ASME, 2018, 140, .	1.2	6

#	Article	IF	Citations
253	Extreme Thinning of Si Wafers for Via-Last and Multi-wafer Stacking Applications. , 2018, , .		6
254	Study of wafer warpage for Fan-Out wafer level packaging: finite element modelling and experimental validation. , 2019, , .		6
255	A Novel Intermetallic Compound Insertion Bonding to Improve Throughput for Sequential 3-D Stacking. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 669-678.	1.4	6
256	Demonstration of a collective hybrid die-to-wafer integration using glass carrier. , 2021, , .		6
257	System exploration and technology demonstration of 3D Wafer-to-Wafer integrated STT-MRAM based caches for advanced Mobile SoCs. , 2020, , .		6
258	High TC superconducting thick-films : Process conditions and characterisation of powders and films. Physica C: Superconductivity and Its Applications, 1988, 153-155, 808-809.	0.6	5
259	Evaluation of structural degradation in packaged semiconductor components using a transient thermal characterisation technique. Microelectronics Reliability, 1996, 36, 1807-1810.	0.9	5
260	Thermal fatigue analysis of the flip chip assembly on the polymer stud grid array (PSGA) package. Microelectronics International, 1999, 16, 15-21.	0.4	5
261	Ultra thin electronics for space applications. , 0, , .		5
262	Accurate RF Electrical Characterization of CSPs Using MCM-D Thin Film Technology. IEEE Transactions on Advanced Packaging, 2004, 27, 203-212.	1.7	5
263	Spin-on dielectric liner TSV for 3D wafer level packaging applications. , 2010, , .		5
264	Mechanical characterization of micro-bump for aggressive bump scaling. , 2012, , .		5
265	Impact of barrier integrity on liner reliability in 3D through silicon vias. , 2013, , .		5
266	Investigation of chip-to-chip interconnections for memory-logic communication on 3D interposer technology. , 2014, , .		5
267	Thermal compression bonding of 20 Î¼m pitch micro bumps with pre-applied underfill - Process and reliability. , 2015, , .		5
268	ESD protection design in active-lite interposer for 2.5 and 3D systems-in-package. , 2015, , .		5
269	Modeling the effect of charges in the back side passivation layer on through silicon via (TSV) capacitance after wafer thinning. , 2015, , .		5
270	Demonstration of a novel low cost single material temporary bond solution for high topography substrates based on a mechanical wafer debonding and innovative adhesive removal. , 2015, , .		5

#	Article	IF	Citations
271	Impact of wafer thinning on front-end reliability for 3D integration. , 2016, , .		5
272	Performance and Reliability Impact of Copper Plasticity in Backside TSV-Last Fabrication Process. IEEE Transactions on Device and Materials Reliability, 2016, 16, 402-412.	1.5	5
273	Methodologies to mitigate package induced stresses in the BEOL. , 2016, , .		5
274	The Increasing Role of Polymers in Advanced Packaging - From Stress Buffer Layers to Wafer Level Underfills and Beyond. Journal of Photopolymer Science and Technology = [Fotoporima Konwakai Shi], 2017, 30, 17-24.	0.1	5
275	TSV process-induced MOS reliability degradation. , 2018, , .		5
276	Advances in Temporary Bonding and Release Technology for Ultrathin Substrate Processing and High-Density Fan-Out Device Build-up. , 2018, , .		5
277	First Demonstration of a Low Cost/Customizable Chip Level 3D Printed Microjet Hotspot-Targeted Cooler for High Power Applications. , 2019, , .		5
278	Novel Temporary Bonding and Debonding Solutions Enabling an Ultrahigh Interonnect Density Fo-Wlp Structure Assembly with Quasi-Zero Die Shift. , 2019, , .		5
279	Multi-tier $mathrm{N}=4$ Binary Stacking, combining Face-to-Face and Back-to-Back Hybrid Wafer-to-Wafer Bonding Technology. , 2021, , .		5
280	The unique properties of SiCN as bonding material for hybrid bonding. , 2021, , .		5
281	Sequential-rotation arrays of circularly polarized CPW-fed aperture antennas in the MCM-D technology. , 2000, , .		4
282	Solder parameter sensitivity for CSP life-time prediction using simulation-based optimization method. IEEE Transactions on Electronics Packaging Manufacturing, 2002, 25, 318-325.	1.6	4
283	Accurate RF electrical characterisation of CSPs using MCM-D thin film technology. , 0, , .		4
284	Bonding on Cu: a new stress evaluation approach by Raman spectroscopy. , 0, , .		4
285	Mechanical behavior of BEOL structures containing lowK dielectrics during bonding process. , 0, , .		4
286	Enabling SPICE-type modeling of the thermal properties of 3D-stacked ICs. , 2006, , .		4
287	Recent Advances in 3D Integration at IMEC. Materials Research Society Symposia Proceedings, 2006, 970, 1.	0.1	4
288	The Shear Test as Interface Characterization Tool Applied to the Si-BCB Interface. Journal of Electronic Packaging, Transactions of the ASME, 2009, 131, .	1.2	4

#	Article	IF	Citations
289	Temporary wafer bonding defect impact assessment on substrate thinning: Process enhancement through systematic defect track down. , 2012, , .		4
290	3D stacking using Cu-Cu direct bonding for 40um pitch and beyond. , 2012, , .		4
291	Thermo mechanical challenges for processing and packaging stacked ultrathin wafers. , 2013, , .		4
292	Metrology and inspection challenges for manufacturing 3D stacked IC's. , 2013, , .		4
293	Cost components for 3D system integration. , 2014, , .		4
294	Temporary bonding for High-topography Applications: Spin-on Material Versus Dry Film. , 2014, , .		4
295	Material technology for 2.5D/3D package. , 2015, , .		4
296	Analysis of copper plasticity impact in TSV-middle and backside TSV-last fabrication processes. , 2015, , .		4
297	Fast and Accurate Modelling of Large TSV Arrays in 3D-ICs Using a 3D Circuit Model Validated Against Full-Wave FEM Simulations and RF Measurements. , 2016, , .		4
298	Technology optimization for high bandwidth density applications on 3D interposer. , 2016, , .		4
299	Fine Pitch Rapid Heat Self-Aligned Assembly and Liquid-Mediated Direct Bonding of Si Chips. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2016, 6, 946-953.	1.4	4
300	Growth rate of IMC in the binary sytems of Co/Sn and Cu/Sn. , 2017, , .		4
301	Characterization of inorganic dielectric layers for low thermal budget wafer-to-wafer bonding. , 2017, , .		4
302	Defect localization of metal interconnection lines in 3-dimensional through-silicon-via structures by differential scanning photocapacitance microscopy. Applied Physics Letters, 2018, 112, 071904.	1.5	4
303	TCB optimization for stacking large thinned dies with 40 and 20 Î¼m pitch microbumps. , 2018, , .		4
304	Inductive Links for 3D Stacked Chip-to-Chip Communication. , 2019, , .		4
305	A novel iso-thermal intermetallic compound insertion bonding approach to improve throughput for 3D die to wafer stacking. , 2020, , .		4
306	Power from Below: Buried Interconnects Will Help Save Moore's Law. IEEE Spectrum, 2021, 58, 46-51.	0.5	4

#	Article	IF	Citations
307	3D Heterogeneous Package Integration of Air/Magnetic Core Inductor: 89%-Efficiency Buck Converter with Backside Power Delivery Network. , 2020, , .		4
308	Carrier Systems for Collective Die-to-Wafer Bonding. , 2022, , .		4
309	Low temperature backside damascene processing on temporary carrier wafer targeting 7Î¼m and 5Î¼m pitch microbumps for N equal and greater than 2 die to wafer TCB stacking. , 2022, , .		4
310	Electromigration: Investigation of heterogeneous systems. Microelectronics Reliability, 1993, 33, 1141-1157.	0.9	3
311	Thermal fatigue reliability analysis of redistributed flip chip assemblies. , 0, , .		3
312	Galerkin versus razor-blade testing in the method of moments formulation for multiconductor transmission lines. International Journal of RF and Microwave Computer-Aided Engineering, 2000, 10, 132-138.	0.8	3
313	Residual thermomechanical stresses in thinned-chip assemblies. IEEE Transactions on Components and Packaging Technologies, 2000, 23, 673-679.	1.4	3
314	Parametric compact models for flip chip assemblies. IEEE Transactions on Components and Packaging Technologies, 2000, 23, 555-561.	1.4	3
315	Pulsed DC Sputtered Aluminum Nitride: A Novel Approach To Control Stress And C-axis Orientation. Materials Research Society Symposia Proceedings, 2004, 833, 63.	0.1	3
316	Analytical Thermo-Mechanical Model for Non-Underfilled Area Array Flip Chip Assemblies. Journal of Electronic Packaging, Transactions of the ASME, 2004, 126, 351-358.	1.2	3
317	Active Electrode Arrays by Chip Embedding in a Flexible Silicone Carrier. , 2006, 2006, 2811-5.		3
318	Constant Impedance Scaling Paradigm for Scaling LC transmission lines. , 0, , .		3
319	Design and Integration Technology for Miniature Medical Microsystems. , 2008, , .		3
320	Ultra thin die embedding technology with 20μm-pitch interconnection. , 2010, , .		3
321	In-line metrology and inspection for process control during 3D stacking of IC's. , 2012, , .		3
322	Underfill material screening and process characterization for 3D stacking. , 2012, , .		3
323	Cu-Cu hybrid bonding as option for 3D IC stacking. , 2012, , .		3
324	Through-silicon via technology for three-dimensional integrated circuit manufacturing. , 2012, , .		3

#	Article	IF	Citations
325	Developing underfill process in screening of no-flow underfill and wafer-applied underfill materials for 3D stacking. , 2013, , .		3
326	Analysis of 3D interconnect performance: Effect of the Si substrate resistivity. , 2014, , .		3
327	Convolution based compact thermal model application to the evaluation of the thermal impact of die to die interface including interconnections. , 2014, , .		3
328	Development and Evaluation of Photodefinable Wafer Level Underfill. Journal of Photopolymer Science and Technology = [Fotoporima Konwakai Shi], 2015, 28, 229-232.	0.1	3
329	An Efficient Bump Pad Design to Mitigate the Flip Chip Package Induced Stress. , 2015, , .		3
330	Impact of backside processing on C-V characteristics of TSV capacitors in 3D stacked IC process flows. , 2015, , .		3
331	3D-SoC integration utilizing high accuracy wafer level bonding. , 2016, , .		3
332	On the feasibility of die-to-wafer inorganic dielectric bonding. , 2016, , .		3
333	Surface Treatment to Enable Low Temperature and Pressure Copper Direct Bonding. , 2016, , .		3
334	High-density and low-leakage novel embedded 3D MIM capacitor on Si interposer. , 2016, , .		3
335	Lock-in thermal laser stimulation for non-destructive failure localization in 3-D devices. Microelectronics Reliability, 2017, 76-77, 188-193.	0.9	3
336	Investigation of Co Thin Film as Buffer Layer Applied to Cu/Sn Eutectic Bonding and UBM With Sn, SnCu, and SAC Solders Joints. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2017, 7, 1899-1905.	1.4	3
337	A Unique Temporary Bond Solution Based on a Polymeric Material Tacky at Room Temperature and Highly Thermally Resistant Application Extension from 3D-SIC to FO-WLP. , 2017, , .		3
338	A study on substrate noise coupling among TSVs in 3D chip stack. IEICE Electronics Express, 2018, 15, 20180460-20180460.	0.3	3
339	Thermal Performance Comparison of Advanced 3D Packaging Concepts for Logic and Memory Integration in Mobile Cooling Conditions. , 2018, , .		3
340	Extreme Thinned-Wafer Bonding Using Low Temperature Curable Polyimide for Advanced Wafer Level Integrations. , 2018, , .		3
341	A High-Bandwidth Fine-Pitch 2.57Tbps/mm In-package Communication Link Achieving 48fJ/bit/mm Efficiency. , 2019, , .		3
342	A Novel Resistance Measurement Methodology for $In~Situ$ UBM/Solder Interfacial Reaction Monitoring. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 30-38.	1.4	3

#	Article	IF	Citations
343	Thermal analysis of 3D functional partitioning for high-performance systems. , 2021, , .		3
344	RF Technologies and Systems. , 2009, , 63-84.		3
345	Characterization of Silicon Carbon Nitride for Low Temperature Wafer-to-Wafer Direct Bonding. ECS Transactions, 2020, 98, 21-31.	0.3	3
346	84%-Efficiency Fully Integrated Voltage Regulator for Computing Systems Enabled by 2.5-D High-Density MIM Capacitor. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 661-665.	2.1	3
347	A step towards MCM design automation. , 0, , .		2
348	<title>New ultrathin 3D integration technique: technological and thermal investigations</title>. , 2000, , .		2
349	Trends in packaging and high density interconnection. , 2000, , .		2
350	Distributed circuit models for near-CSP interconnects. , 0, , .		2
351	Electrical characterisation of BGA package for RF applications. Microelectronics International, 2002, 19, 13-18.	0.4	2
352	Highâ€QRF inductors on 20â€‰Î©.cm silicon realized through waferâ€level packaging techniques. Microelectronics International, 2003, 20, 26-30.	0.4	2
353	Accurate broadband parameter extraction methodology for s-parameter measurements. , 0, , .		2
354	Analysis and Modeling of Power Grid Transmission lines. , 2006, , .		2
355	Efficient Link Architecture for On-Chip Serial links and Networks. , 2006, , .		2
356	Process technology for the fabrication of a Chip-in-Wire style packaging. , 2008, , .		2
357	Direct Hybrid Bonding. Integrated Circuits and Systems, 2008, , 1-11.	0.2	2
358	Verifying thermal/thermo-mechanical behavior of a 3D stack — challenges and solutions. , 2010, , .		2
359	Alternative patterning techniques enabling fine pitch interconnection on topography surfaces. , 2010, , .		2
360	Verifying thermal/thermo-mechanical behavior of a 3D stack - challenges and solutions. , 2010, , .		2

#	Article	IF	Citations
361	RF SiP technologies enabling wireless modules. , 2011, , .		2
362	Fine Pitch Micro-Bump Interconnections for Advanced 3D Chip Stacking. ECS Transactions, 2011, 34, 523-528.	0.3	2
363	Thermal mismatch induced reliability issues for Cu filled through-silicon vias. , 2012, , .		2
364	In-tier diagnosis of power domains in 3D TSV ICs. , 2012, , .		2
365	A study on power integrity in a 3D chip stack using dynamic power supply current emulation and power noise monitoring. , 2014, , .		2
366	Reliability of 3D package using wafer level underfill and low CTE epoxy mold compound materials. , 2014, , .		2
367	Room temperature and zero pressure high quality oxide direct bonding for 3D self-aligned assembly. , 2014, , .		2
368	Cu TSV Stress: Avoiding Cu Protrusion and Impact on Devices. , 2014, , 365-378.		2
369	Through silicon via to FinFET noise coupling in 3-D integrated circuits. , 2015, , .		2
370	Reliability study of liner/barrier/seed options for via-middle TSV's with 3 micron diameter and below. , 2015, , .		2
371	A novel structure of MOSFET array to measure ioff-ion with high accuracy and high density. , 2015, , .		2
372	Packaging Material Evaluation for 2.5D/3D TSV Application. Transactions of the Japan Institute of Electronics Packaging, 2016, 9, E16-011-1-E16-011-7.	0.3	2
373	Investigation of TSV noise coupling in 3D-ICs using an experimental validated 3D TSV circuit model including Si substrate effects and TSV capacitance inversion behavior after wafer thinning. , 2016, , .		2
374	Low Warpage Wafer Level Transfer Molding Post 3D Die to Wafer Assembly. , 2016, , .		2
375	Impact of backside process on high aspect ratio via-middle Cu through silicon via reliability. , 2017, , .		2
376	Interface charge trapping induced flatband voltage shift during plasma-enhanced atomic layer deposition in through silicon via. Journal of Applied Physics, 2017, 122, .	1.1	2
377	A novel in-situ resistance measurement to extract IMC resistivity and kinetic parameter for CoSn 3D stacks. , 2017, , .		2
378	Physics of self-aligned assembly at room temperature. Physics of Fluids, 2018, 30, .	1.6	2

#	Article	IF	Citations
379	Etch process modules development and integration in 3D-SOC applications. Microelectronic Engineering, 2018, 196, 38-48.	1.1	2
380	Anomalous ${C}$ â€“ ${V}$ Inversion in TSVs: The Problem and Its Cure. IEEE Transactions on Electron Devices, 2018, 65, 1473-1479.	1.6	2
381	An in-situ resistance measurement to extract IMC resistivity and kinetic parameter of alternative metallurgies for 3D stacking. , 2018, , .		2
382	A Highly Reliable 1Ã—5Î¼m Via-last TSV Module. , 2018, , .		2
383	Improved Staggered Through Silicon Via Inductors for RF and Power Applications. , 2018, , .		2
384	Thermal Management and Processing Optimization for 3D Multi-layer Stacked ICs. , 2019, , .		2
385	System Optimization: High-Frequency Buck Converter With 3-D In-Package Air-Core Inductor. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2022, 12, 401-409.	1.4	2
386	Epitaxial Growth of Active Si on Top of SiGe Etch Stop Layer in View of 3D Device Integration. ECS Journal of Solid State Science and Technology, 2021, 10, 014001.	0.9	2
387	Fine-pitch 3D system integration and advanced CMOS nodes: technology and system design perspective. , 2021, , .		2
388	Cobalt-Tin Intermetallic Compounds as Alternative Surface Finish for Low Temperature Die-to-Wafer Solder Stacking. , 2021, , .		2
389	Broadband permittivity characterization of polymers up to 110GHz using co-planar waveguides. , 2021, , .		2
390	NOZZLE ARRAY SCALING EFFECTS ON THE THERMAL/HYDRAULIC PERFORMANCE OF LIQUID JET IMPINGEMENT COOLERS FOR HIGH PERFORMANCE ELECTRONIC APPLICATIONS. , 2018, , .		2
391	Application of the surface planer process to Cu pillars and wafer support tape for high-coplanarity wafer-level packaging. International Journal of Advanced Manufacturing Technology, 2022, 119, 3427-3435.	1.5	2
392	Design And Sign-off Methodologies For Wafer-To-Wafer Bonded 3D-ICs At Advanced Nodes (invited). , 2021, , .		2
393	Reliability Investigation of W2W Hybrid Bonding Interface: Breakdown Voltage and Leakage Mechanism. , 2022, , .		2
394	A system level approach to a structured MCM design methodology. , 0, , .		1
395	The kinetics of the early stages of electromigration and concurrent temperature induced processes in thin film metallisations studied by means of an in-situ high resolution resistometric technique. Microelectronics Reliability, 1999, 39, 1657-1665.	0.9	1
396	Coplanar Versus Slotline Mode in Exciting CPW-FED Planar Antennas. , 1999, , .		1

#	Article	IF	Citations
397	<title>Residual thermomechanical stresses in ultrathin chip stack technology</title>. , 2000, , .		1
398	A Modified Electromigration Test Structure for Flip Chip Interconnections. IEEE Transactions on Components and Packaging Technologies, 2006, 29, 508-511.	1.4	1
399	Use of Polymer Liners for 3D-WLP TSVs: Process, Reliability and Cost. ECS Transactions, 2010, 33, 41-54.	0.3	1
400	3D Stacking Heterogeneous Integration for Devices and Modules. ECS Transactions, 2012, 44, 721-726.	0.3	1
401	Wafer thinning and back side processing to enable 3D stacking. , 2012, , .		1
402	Process development to enable die sorting and 3D IC stacking. , 2012, , .		1
403	Photosensitive insulation coating for a copper redistribution layer process. , 2014, , .		1
404	Challenges and solutions on pre-assembly processes for thinned 3D wafers with micro-bumps on the backside. , 2014, , .		1
405	2D vs 3D integration: Architecture-technology co-design for future mobile MPSoC platforms. , 2014, , .		1
406	Thinning, Via Reveal, and Backside Processing - Overview. , 2014, , 191-206.		1
407	Stress and bowing engineering in passive silicon interposer. , 2015, , .		1
408	Continuity and reliability assessment of a scalable 3Ã—50Î¼m and 2Ã—40Î¼m via-middle TSV module. , 2016, , .		1
409	Impact of ELD layers in mechanical properties of microbumps for 3D stacking. , 2016, , .		1
410	Liquid mediated direct bonding and bond propagation. , 2016, , .		1
411	Convolution-Based Fast Thermal Model for 3-D-ICs: Transient Experimental Validation. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2017, , 1-16.	1.4	1
412	Impact of via density and passivation thickness on the mechanical integrity of advanced Back-End-Of-Line interconnects. Microelectronics Reliability, 2017, 79, 297-305.	0.9	1
413	A Simple and Efficient RF Technique for TSV Characterization. , 2017, , .		1
414	Influence of Composition of SiCN Film for Surface Activated Bonding. ECS Transactions, 2018, 86, 159-168.	0.3	1

#	Article	IF	Citations
415	Enhanced Cu pillar design to reduce thermomechanical stress induced during flip chip assembly. Microelectronics Reliability, 2018, 87, 97-105.	0.9	1
416	Novel Failure Analysis Techniques for 1.8 Âµm Pitch Wafer-to-Wafer Bonding. , 2018, , .		1
417	Thermal Analysis of a 3D Flip-chip Fan-out Wafer Level Package (fcFOWLP) for High Bandwidth 3D Integration. , 2019, , .		1
418	Pre-bonding Characterization of SiCN Enabled Wafer Stacking. , 2019, , .		1
419	Process Complexity and Cost Considerations of Multi-Layer Die Stacks. , 2019, , .		1
420	RF characterization of mold compound materials and high-Q integrated passives using fan-out wafer-level packaging technology. , 2019, , .		1
421	Localization of Electrical Defects in Hybrid Bonding Interconnect Structures by Scanning Photocapacitance Microscopy. IEEE Transactions on Instrumentation and Measurement, 2021, 70, 1-7.	2.4	1
422	A study on IMC morphology and integration flow for low temperature and high throughput TCB down to $10mu mathrm{m}$ pitch microbumps. , 2021, , .		1
423	Influence Of Solder Joint Shape On The Thermo-Mechanical Reliability Of CSP's. Journal of Microelectronics and Electronic Packaging, 2004, 1, 53-63.	0.8	1
424	Electro-migration behavior of Pb-free Flip Chip Bumps. Journal of Microelectronics and Electronic Packaging, 2006, 3, 32-36.	0.8	1
425	Packaging and Assembly Challenges for 2.5D/3D Devices. Additional Conferences (Device Packaging) Tj ETQq1 1 0.784314 rgBT /Overlo	0.2	1
426	ELD NiB for microbumps passivation and wirebonding. , 2020, , .		1
427	Tbps/mm bandwidth for chip-to-chip communication using fine pitch damascene RDL. , 2020, , .		1
428	Modeling of Buck Converter with 3D Air-Core Inductor. , 2020, , .		1
429	Fundamental study of IMC grains at low anneal temperature. , 2022, , .		1
430	Broadband Characterization of Polymers under Reliability Stresses and Impact of Capping Layer. , 2022, , .		1
431	Interconnect technologies for multi-chip modules: high frequency characterization and loss analysis. Microelectronic Engineering, 1992, 19, 563-566.	1.1	0
432	Electromigration at goldâ€"aluminium interfaces and in thin aluminium tracks. Quality and Reliability Engineering International, 1992, 8, 253-258.	1.4	0

#	Article	IF	Citations
433	Design of test modules for the analysis of MCM interconnects. , 1996, , .		0
434	Realisation of a DECT VCO circuit with MCM-D technology. , 1999, , .		0
435	Performance prediction of printed lumped inductors on a multilayer medium. , 2000, , .		0
436	Analysis and design of two types of microwave baluns. , 0, , .		0
437	An optimized process for the production of advanced planar wire grid plates as detectors for high energy physics experiments. Sensors and Actuators A: Physical, 2001, 93, 76-83.	2.0	0
438	Mixed assembly on PCB of wide variety components (MCM-D, SMDs, bare dies) using wire bonding and SMT. , 0, , .		0
439	Advantage of In-situ over Ex-situ techniques as reliability tool: Aging kinetics of Imecâ€™s MCM-D discrete passives devices.. Microelectronics Reliability, 2003, 43, 1785-1790.	0.9	0
440	Process and Material Requirements for Successful Heterogonous Passive Component Integration in RF System. Materials Research Society Symposia Proceedings, 2006, 969, .	0.1	0
441	Process and Material Requirements for Successful Heterogonous Passive Component Integration in RF System. Materials Research Society Symposia Proceedings, 2006, 969, 1.	0.1	0
442	Probabilistic design approach for integrated passive devices in RF applications. , 2008, , .		0
443	Area Optimized Thin Film Coupled Inductor Band Pass Filters with Integrated Baluns. , 2008, , .		0
444	Chip ultra-thinning and embedding technology for autonomous sensors array applications. , 2009, , .		0
445	Advanced Technologies for In-Line and Post-Processed TSV Integration. ECS Transactions, 2009, 18, 695-700.	0.3	0
446	Shaping interconnect technology for an interconnected society. , 2010, , .		0
447	Fabrication and Electrical Evaluation of Via Last Polymer Liner TSVs. Journal of Microelectronics and Electronic Packaging, 2010, 7, 125-130.	0.8	0
448	Metrology and inspection rquirements for 3D stacking of ICs. , 2012, , .		0
449	IC-Package Interaction. , 2013, , .		0
450	Picking large thinned dies with high topography on both sides. , 2014, , .		0

#	Article	IF	Citations
451	Cu-Cu insertion bonding technique using photosensitive polymer as WLUF. , 2014, , .		0
452	Metrology and Inspection Requirements for Successful Stacking of Integrated Circuits. IEEE Transactions on Semiconductor Manufacturing, 2014, 27, 370-376.	1.4	0
453	Microstructure simulation of grain growth in Cu Through Silicon Via using phase-field modeling. , 2014, , .		0
454	Enabling pre-assembly process of 3D wafers with high topography at the backside. , 2015, , .		0
455	Comparison of properties of thermo-compression bonded 3D stacks using a liquid and a dry-film wafer level underfills. , 2015, , .		0
456	An alternative 3D packaging route through wafer reconstruction. , 2015, , .		0
457	Thermal experimental and modeling analysis of high power 3D packages. , 2015, , .		0
458	Cost Comparison of Different TSV Implementation Options. , 2016, , .		0
459	Alternative Cu pillar bumps design to reduce thermomechanical stress induced during flip chip assembly. , 2017, , .		0
460	3D stacking cobalt and nickel microbumps and kinetics of corresponding IMCs at low temperatures. , 2017, , .		0
461	Assembly Technology for Fine Pitch Bumps Using Photodefinable Wafer-Level Underfill. Journal of Smart Processing, 2017, 6, 149-155.	0.0	0
462	Characterization of Optical End-Point Detection for Via Reveal Processing. , 2018, , .		0
463	Defect Identification in Bonding Surface Layers by Positron Annihilation Spectroscopy. , 2019, , .		0
464	New approach to apply 1,2,3-benzotriazole as a capping layer on UBMs for 3D TCB stacking and investigation of oxidation protection and solder wetting. , 2019, , .		0
465	Integrated magnetic cores in FOWLP and their applications. , 2020, , .		0
466	Process development and characterization of 3D multi-die stacking. , 2020, , .		0
467	A Novel Method for Characterization of Ultralow Viscosity NCF Layers Using TCB for 3D Assembly. Journal of Microelectronics and Electronic Packaging, 2021, 18, 12-20.	0.8	0
468	Heterogeneous Integration of Passive Components for the Realization of RF-System-in-Packages. , 2008, , 3-14.		0

#	Article	IF	Citations
469	Use of Wafer Applied Underfill for 3D Stacking. Journal of Microelectronics and Electronic Packaging, 2012, 9, 10-18.	0.8	0
470	Evaluation of UBM oxidation through air exposure and heating and effectiveness of wet and plasma cleaning on solder joint formation during TCB. , 2020, , .		0
471	A novel method for characterization of Ultra Low Viscosity NCF layers using TCB for 3D Assembly. International Symposium on Microelectronics, 2020, 2020, 000185-000191.	0.3	0
472	Epitaxial Growth of Active Si on Top of SiGe Etch Stop Layer in View of 3D Device Integration. ECS Transactions, 2020, 98, 157-166.	0.3	0