Balwinder Raj

List of Publications by Year
in descending order

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49 papers	945 citations	430874 18 h-index	526287 27 g-index
49 all docs	49 docs citations	49 times ranked	323 citing authors

#	Article	IF	Citations
1	Label Free Detection of Biomolecules Using Charge-Plasma-Based Gate Underlap Dielectric Modulated Junctionless TFET. Journal of Electronic Materials, 2018, 47, 4683-4693.	2.2	78
2	Parametric Variation Analysis of Symmetric Double Gate Charge Plasma JLTFET for Biosensor Application. IEEE Sensors Journal, 2018, 18, 6070-6077.	4.7	70
3	Design, Simulation and Performance Analysis of JLTFET Biosensor for High Sensitivity. IEEE Nanotechnology Magazine, 2019, 18, 567-574.	2.0	69
4	INDEP approach for leakage reduction in nanoscale CMOS circuits. International Journal of Electronics, 2015, 102, 200-215.	1.4	43
5	Analytical modeling of split-gate junction-less transistor for a biosensor application. Sensing and Bio-Sensing Research, 2018, 18, 31-36.	4.2	38
6	Design and Analysis of a Heterojunction Vertical t-Shaped Tunnel Field Effect Transistor. Journal of Electronic Materials, 2019, 48, 6253-6260.	2.2	38
7	Design and Investigation of 7T2M-NVSRAM With Enhanced Stability and Temperature Impact on Store/Restore Energy. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1322-1328.	3.1	37
8	Design and Analysis of Dual Source Vertical Tunnel Field Effect Transistor for High Performance. Transactions on Electrical and Electronic Materials, 2020, 21, 74-82.	1.9	34
9	Modeling and simulation analysis of SiGe heterojunction Double Gate Vertical t-shaped tunnel FET. Superlattices and Microstructures, 2020, 142, 106496.	3.1	32
10	PVT variations aware low leakage INDEP approach for nanoscale CMOS circuits. Microelectronics Reliability, 2014, 54, 90-99.	1.7	31
11	Compact channel potential analytical modeling of DG-TFET based on Evanescent-mode approach. Journal of Computational Electronics, 2015, 14, 820-827.	2.5	30
12	Analysis of I_{ON} and Ambipolar Current for Dual-Material Gate-Drain Overlapped DG-TFET. Journal of Nanoelectronics and Optoelectronics, 2016, 11, 323-333.	0.5	28
13	Temperature-Dependent Modeling and Performance Evaluation of Multi-Walled CNT and Single-Walled CNT as Global Interconnects. Journal of Electronic Materials, 2015, 44, 4825-4835.	2.2	27
14	Comparative analysis of photovoltaic technologies for high efficiency solar cell design. Superlattices and Microstructures, 2021, 153, 106861.	3.1	27
15	Two-dimensional analytical modeling of the surface potential and drain current of a double-gate vertical t-shaped tunnel field-effect transistor. Journal of Computational Electronics, 2020, 19, 1154-1163.	2.5	26
16	Analytical modeling for the estimation of leakage current and subthreshold swing factor of nanoscale double gate FinFET device. Microelectronics International, 2009, 26, 53-63.	0.6	24
17	Modeling of Mean Barrier Height Levying Various Image Forces of Metalâ€“Insulatorâ€“Metal Structure to Enhance the Performance of Conductive Filament Based Memristor Model. IEEE Nanotechnology Magazine, 2018, 17, 268-275.	2.0	23
18	Design and analysis of a gate-all-around CNTFET-based SRAM cell. Journal of Computational Electronics, 2018, 17, 138-145.	2.5	20

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19	An analytical modeling of charge plasma based Tunnel Field Effect Transistor with impacts of gate underlap region. Superlattices and Microstructures, 2020, 142, 106512.	3.1	20
20	Quantum mechanical analytical modeling of nanoscale DG FinFET: evaluation of potential, threshold voltage and source/drain resistance. Materials Science in Semiconductor Processing, 2013, 16, 1131-1137.	4.0	17
21	Influence of temperature on MWCNT bundle, SWCNT bundle and copper interconnects for nanoscaled technology nodes. Journal of Materials Science: Materials in Electronics, 2015, 26, 6134-6142.	2.2	17
22	Analytical modeling and simulation analysis of T-shaped III-V heterojunction vertical T-FET. Superlattices and Microstructures, 2020, 147, 106717.	3.1	17
23	Performance and analysis of temperature dependent multi-walled carbon nanotubes as global interconnects at different technology nodes. Journal of Computational Electronics, 2015, 14, 469-476.	2.5	15
24	Analytical Modelling and Simulation of Si-Ge Hetero-Junction Dual Material Gate Vertical T-Shaped Tunnel FET. Silicon, 2021, 13, 1139-1150.	3.3	15
25	Design and analysis of double-gate junctionless vertical TFET for gas sensing applications. Applied Physics A: Materials Science and Processing, 2021, 127, 1.	2.3	15
26	Design optimisation of junctionless TFET biosensor for high sensitivity. Advances in Natural Sciences: Nanoscience and Nanotechnology, 2019, 10, 045001.	1.5	14
27	Circuit Compatible Model for Electrostatic Doped Schottky Barrier CNTFET. Journal of Electronic Materials, 2016, 45, 5381-5390.	2.2	12
28	Analysis of electrostatic doped Schottky barrier carbon nanotube FET for low power applications. Journal of Materials Science: Materials in Electronics, 2017, 28, 1762-1768.	2.2	12
29	Analytical and Compact Modeling Analysis of a SiGe Hetero-Material Vertical L-Shaped TFET. Silicon, 2022, 14, 2135-2145.	3.3	11
30	Design and comparative analysis of various planar perovskite solar cells through numerical simulation using different HTLs to improve efficiency. Optical Materials, 2022, 126, 112221.	3.6	11
31	Surface Potential Modeling and Simulation Analysis of Dopingless TFET Biosensor. Silicon, 2022, 14, 2147-2156.	3.3	10
32	Design and optimization of junctionless-based devices with noise reduction for ultra-high frequency applications. Applied Physics A: Materials Science and Processing, 2020, 126, 1.	2.3	9
33	Analysis of ONOFIC Technique Using SiGe Heterojunction Double Gate Vertical TFET for Low Power Applications. Silicon, 2021, 13, 2115-2124.	3.3	9
34	Improved Sensitivity of Dielectric Modulated Junctionless Transistor for Nanoscale Biosensor Design. Sensor Letters, 2020, 18, 328-333.	0.4	8
35	Compact model for ballistic single wall CNTFET under quantum capacitance limit. Journal of Semiconductors, 2016, 37, 104001.	3.7	7
36	RF analysis of intercalated graphene nanoribbon-based global-level interconnects. Journal of Computational Electronics, 2020, 19, 1002-1013.	2.5	7

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37	Dual-Material Gate-Drain Overlapped DG-TFET Device for Low Leakage Current Design. Silicon, 2021, 13, 1599-1607.	3.3	7
38	Simulations and Modeling of TFET for Low Power Design. Advances in Systems Analysis, Software Engineering, and High Performance Computing Book Series, 2016, , 640-667.	0.5	7
39	Design and Analysis of Junctionless Based Symmetric Nanogap-Embedded TFET Biosensor. IETE Journal of Research, 2023, 69, 2655-2663.	2.6	6
40	Methods for Integration of III-V Compound and Silicon Multijunction for High Efficiency Solar Cell Design. Silicon, 2022, 14, 9797-9804.	3.3	6
41	Detection of Biomolecules Using Charge-Plasma Based Gate Underlap Dielectric Modulated Dopingless TFET. Transactions on Electrical and Electronic Materials, 2020, 21, 528-535.	1.9	4
42	In1â€‰â^'â€‰xGaxAs Double Metal Gate-Stacking Cylindrical Nanowire MOSFET for Highly Sensitive Photo Detector. Silicon, 2022, 14, 3535-3541.	3.3	4
43	Comparative Analysis of OFETs Materials and Devices for Sensor Applications. Silicon, 2022, 14, 4463-4471.	3.3	4
44	Junctionless Silicon Nanotube Tunnel Field Effect Transistor Based Resistive Temperature Detector. Silicon, 0, , 1.	3.3	3
45	Surface Potential and Drain Current 2D Analytical Modeling of Low Power Double Gate Tunnel FET. Transactions on Electrical and Electronic Materials, 2021, 22, 764.	1.9	2
46	Comparative radioâ€frequency and crosstalk analysis of carbonâ€based nanoâ€interconnects. IET Circuits, Devices and Systems, 2021, 15, 493-503.	1.4	1
47	Memristive Fractional-Order Nonlinear Model for Circuit Design. , 2018, , 421-449.		0
48	Simulation Study of Linearly Graded Binary Metal Alloy PÎ±Q1-Î± Gate TFET Device for Realization of Boolean Functions. Silicon, 0, , 1.	3.3	0
49	Design of Spintronics Based MRAM with Comparative Analysis of MJT and Silicon MOSFET. Silicon, 0, , 1.	3.3	0