Nikil Dutt

List of Publications by Year in Descending Order

333 papers	3,918 citations	29 h-index	47 g-index
394 ext. papers	4,968 ext. citations	2.5 avg, IF	5.63 L-index

#	Paper	IF	Citations
333	A novel wireless ECG system for prolonged monitoring of multiple zebrafish for heart disease and drug screening studies. *Biosensors and Bioelectronics*, **2022**, 197, 113808	11.8	1
332	. *IEEE Transactions on Parallel and Distributed Systems*, **2022**, 33, 288-301	3.7	8
331	Digital Health-Enabled Community-Centered Care: Scalable Model to Empower Future Community Health Workers Using Human-in-the-Loop Artificial Intelligence.. *JMIR Formative Research*, **2022**, 6, e29535	2.5	1
330	A Micro-Level Analysis of Physiological Responses to COVID-19: Continuous Monitoring of Pregnant Women in California.. *Frontiers in Public Health*, **2022**, 10, 808763	6	0
329	Reflecting on Self-Aware Systems-on-Chip **2021**, 79-95		0
328	NeuroXplorer 1.0: An Extensible Framework for Architectural Exploration with Spiking Neural Networks **2021**,		4
327	An Interpretable Machine Learning Model Enhanced Integrated CPU-GPU DVFS Governor. *Transactions on Embedded Computing Systems*, **2021**, 20, 1-28	1.8	1
326	Exploiting Memory Resilience for Emerging Technologies: An Energy-Aware Resilience Exemplar for STT-RAM Memories. *Embedded Systems*, **2021**, 505-526		
325	Assessing the Mental Health of Emerging Adults Through a Mental Health App: Protocol for a Prospective Pilot Study. *JMIR Research Protocols*, **2021**, 10, e25775	2	4
324	Long-Term IoT-Based Maternal Monitoring: System Design and Evaluation. *Sensors*, **2021**, 21,	3.8	7
323	The Causality Inference of Public Interest in Restaurants and Bars on Daily COVID-19 Cases in the United States: Google Trends Analysis. *JMIR Public Health and Surveillance*, **2021**, 7, e22880	11.4	3
322	Pain Recognition With Electrocardiographic Features in Postoperative Patients: Method Validation Study. *Journal of Medical Internet Research*, **2021**, 23, e25079	7.6	3
321	Pain Assessment Tool With Electrodermal Activity for Postoperative Patients: Method Validation Study. *JMIR MHealth and UHealth*, **2021**, 9, e25258	5.5	5
320	Using Multimodal Assessments to Capture Personalized Contexts of College Student Well-being in 2020: Case Study. *JMIR Formative Research*, **2021**, 5, e26186	2.5	0
319	A Technology-Based Pregnancy Health and Wellness Intervention (Two Happy Hearts): Case Study. *JMIR Formative Research*, **2021**, 5, e30991	2.5	0
318	Exploring computation offloading in IoT systems. *Information Systems*, **2021**, 101860	2.7	1
317	Predicting Failures in Embedded Systems Using Long Short-Term Inference. *IEEE Embedded Systems Letters*, **2021**, 13, 85-89	1	

316	pyEDA: An Open-Source Python Toolkit for Pre-processing and Feature Extraction of Electrodermal Activity. *Procedia Computer Science*, **2021**, 184, 99-106	1.6	3
315	Edge-Assisted Control for Healthcare Internet of Things. *ACM Transactions on Internet of Things*, **2021**, 2, 1-21	2.2	4
314	SEAMS. *Transactions on Embedded Computing Systems*, **2021**, 20, 1-26	1.8	0
313	Intelligent Management of Mobile Systems Through Computational Self-Awareness. *Advances in Systems Analysis, Software Engineering, and High Performance Computing Book Series*, **2021**, 41-73	0.4	2
312	Personalized Stress Monitoring using Wearable Sensors in Everyday Settings. *Annual International Conference of the IEEE Engineering in Medicine and Biology Society IEEE Engineering in Medicine and Biology Society Annual International Conference*, **2021**, 2021, 7332-7335	0.9	2
311	Investigation of Machine Learning and Deep Learning Approaches for Detection of Mild Traumatic Brain Injury from Human Sleep Electroencephalogram. *Annual International Conference of the IEEE Engineering in Medicine and Biology Society IEEE Engineering in Medicine and Biology Society Annual International Conference*, **2021**, 2021, 6134-6137	0.9	
310	CryptoPIM: In-memory Acceleration for Lattice-based Cryptographic Hardware **2020**,		4
309	Data Reuse for Accelerated Approximate Warps. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 4623-4634	2.5	3
308	Optimizing Energy Efficiency of Wearable Sensors Using Fog-assisted Control **2020**, 245-268		2
307	. *Proceedings of the IEEE*, **2020**, 108, 1027-1046	14.3	3
306	Objective stress monitoring based on wearable sensors in everyday settings. *Journal of Medical Engineering and Technology*, **2020**, 44, 177-189	1.8	9
305	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 4385-4398	2.5	2
304	HCI and mHealth Wearable Tech: A Multidisciplinary Research Challenge **2020**,		4
303	Context-Aware Sensing via Dynamic Programming for Edge-Assisted Wearable Systems. *ACM Transactions on Computing for Healthcare*, **2020**, 1, 1-25	2.6	3
302	Synthesis of Flexible Accelerators for Early Adoption of Ring-LWE Post-quantum Cryptography. *Transactions on Embedded Computing Systems*, **2020**, 19, 1-17	1.8	4
301	Exploiting Heterogeneous Mobile Architectures Through a Unified Runtime Framework. *IFIP Advances in Information and Communication Technology*, **2020**, 323-344	0.5	
300	Prospective Study Evaluating a Pain Assessment Tool in a Postoperative Environment: Protocol for Algorithm Testing and Enhancement. *JMIR Research Protocols*, **2020**, 9, e17783	2	3
299	Sleep Tracking of a Commercially Available Smart Ring and Smartwatch Against Medical-Grade Actigraphy in Everyday Settings: Instrument Validation Study. *JMIR MHealth and UHealth*, **2020**, 8, e20465	5.5	25

298	Classification of Electroencephalogram in a Mouse Model of Traumatic Brain Injury Using Machine Learning Approaches. *Annual International Conference of the IEEE Engineering in Medicine and Biology Society IEEE Engineering in Medicine and Biology Society Annual International Conference*, **2020**, 2020, 3335-3338	0.9	1
297	An Efficient and Robust Deep Learning Method with 1-D Octave Convolution to Extract Fetal Electrocardiogram. *Sensors*, **2020**, 20,	3.8	7
296	Enabling Resource-Aware Mapping of Spiking Neural Networks via Spatial Decomposition. *IEEE Embedded Systems Letters*, **2020**, 1-1	1	7
295	Exploring Energy Efficient Quantum-resistant Signal Processing Using Array Processors **2020**,		5
294	Self-Adaptive Memory Approximation: A Formal Control Theory Approach. *IEEE Embedded Systems Letters*, **2020**, 12, 33-36	1	2
293	Investigation of Machine Learning Approaches for Traumatic Brain Injury Classification via EEG Assessment in Mice. *Sensors*, **2020**, 20,	3.8	7
292	Goal-Driven Autonomy for Efficient On-chip Resource Management: Transforming Objectives to Goals **2019**,		9
291	Energy-efficient and Reliable Wearable Internet-of-Things through Fog-Assisted Dynamic Goal Management. *Procedia Computer Science*, **2019**, 151, 493-500	1.6	8
290	A Real-time PPG Quality Assessment Approach for Healthcare Internet-of-Things. *Procedia Computer Science*, **2019**, 151, 551-558	1.6	24
289	The Case for Exploiting Underutilized Resources in Heterogeneous Mobile Architectures **2019**,		2
288	Post-Quantum Lattice-Based Cryptography Implementations. *ACM Computing Surveys*, **2019**, 51, 1-41	13.4	63
287	Hierarchical adaptive Multi-objective resource management for many-core systems. *Journal of Systems Architecture*, **2019**, 97, 416-427	5.5	2
286	The power impact of hardware and software actuators on self-adaptable many-core systems. *Journal of Systems Architecture*, **2019**, 97, 42-53	5.5	
285	Small Memory Footprint Neural Network Accelerators **2019**,		6
284	. *IEEE Transactions on Computers*, **2019**, 68, 1174-1189	2.5	5
283	ARGA **2019**,		8
282	Neural correlates of sparse coding and dimensionality reduction. *PLoS Computational Biology*, **2019**, 15, e1006908	5	29
281	. *IEEE Access*, **2019**, 7, 93433-93447	3.5	19

280	Dynamic Computation Migration at the Edge **2019**,		3
279	HESSLE-FREE. *Transactions on Embedded Computing Systems*, **2019**, 18, 1-19	1.8	4
278	SOSA **2019**,		8
277	On-Chip Dynamic Resource Managemen. *Foundations and Trends in Electronic Design Automation*, **2019**, 13, 1-144	1	3
276	Flexible NTT Accelerators for RLWE Lattice-Based Cryptography **2019**,		2
275	**2019**,		2
274	A Framework to Explore Workload-Specific Performance and Lifetime Trade-offs in Neuromorphic Computing. *IEEE Computer Architecture Letters*, **2019**, 18, 149-152	1.8	17
273	An Edge-Assisted and Smart System for Real-Time Pain Monitoring **2019**,		7
272	The information processing factory **2019**,		3
271	HDGM: Hierarchical Dynamic Goal Management for Many-Core Resource Allocation. *IEEE Embedded Systems Letters*, **2018**, 10, 61-64	1	5
270	. *IEEE Transactions on Multi-Scale Computing Systems*, **2018**, 4, 944-951		4
269	SPECTR **2018**,		20
268	Synergistic CPU-GPU Frequency Capping for Energy-Efficient Mobile Games. *Transactions on Embedded Computing Systems*, **2018**, 17, 1-24	1.8	6
267	Unsupervised heart-rate estimation in wearables with Liquid states and a probabilistic readout. *Neural Networks*, **2018**, 99, 134-147	9.1	36
266	MEMCOP: memory-aware co-operative power management governor for mobile games. *Design Automation for Embedded Systems*, **2018**, 22, 95-116	0.6	3
265	Approximation-aware coordinated power/performance management for heterogeneous multi-cores **2018**,		3
264	Thermal-Aware Task Mapping on Dynamically Reconfigurable Network-on-Chip Based Multiprocessor System-on-Chip. *IEEE Transactions on Computers*, **2018**, 67, 1818-1834	2.5	16
263	SPECTR. *ACM SIGPLAN Notices*, **2018**, 53, 169-183	0.2	3

244	. *IEEE Embedded Systems Letters*, **2017**, 9, 109-112	1	3
243	Trends, challenges and needs for lattice-based cryptography implementations **2017**,		8
242	Quality-configurable memory hierarchy through approximation **2017**,		2
241	Self-Awareness in Systems on Chip⸺A Survey. *IEEE Design and Test*, **2017**, 34, 8-26	1.4	20
240	Exploring fast and slow memories in HMP core types **2017**,		1
239	**2017**,		4
238	ML-Gov **2017**,		8
237	Architecture and Cross-Layer Design Space Exploration **2017**, 247-270		
236	Microarchitecture-Level SoC Design **2017**, 867-913		
235	Automatic management of Software Programmable Memories in Many-core Architectures. *IET Computers and Digital Techniques*, **2016**, 10, 288-298	0.9	5
234	SPARTA **2016**,		49
233	SPMPool. *Transactions on Embedded Computing Systems*, **2016**, 16, 1-27	1.8	5
232	Conquering MPSoC complexity with principles of a self-aware information processing factory **2016**,		5
231	Self-Awareness in Cyber-Physical Systems **2016**,		8
230	Toward Smart Embedded Systems. *Transactions on Embedded Computing Systems*, **2016**, 15, 1-27	1.8	49
229	Co-Cap **2016**,		6
228	Microarchitecture-Level SoC Design **2016**, 1-46		
227	Architecture and Cross-Layer Design Space Exploration **2016**, 1-24		

226	Approximation knob **2016**,		10
225	On Detecting and Using Memory Phases in Multimedia Systems **2016**,		2
224	Cross-layer virtual/physical sensing and actuation for resilient heterogeneous many-core SoCs **2016**,		1
223	HiCAP **2016**,		11
222	3D Visual Response Properties of MSTd Emerge from an Efficient, Sparse Population Code. *Journal of Neuroscience*, **2016**, 36, 8399-415	6.6	9
221	Models, abstractions, and architectures **2015**,		10
220	Thermal sensor allocation for SoCs based on temperature gradients **2015**,		3
219	Orchestrated application quality and energy storage management in solar-powered embedded systems **2015**,		2
218	Using a Flexible Fault-Tolerant Cache to Improve Reliability for Ultra Low Voltage Operation. *Transactions on Embedded Computing Systems*, **2015**, 14, 1-24	1.8	4
217	Cross-Layer Exploration of Heterogeneous Multicore Processor Configurations **2015**,		6
216	Large-Scale Spiking Neural Networks using Neuromorphic Hardware Compatible Models. *ACM Journal on Emerging Technologies in Computing Systems*, **2015**, 11, 1-18	1.7	13
215	ViPZonE: Hardware Power Variability-Aware Virtual Memory Management for Energy Savings. *IEEE Transactions on Computers*, **2015**, 64, 1483-1496	2.5	6
214	Protecting caches against multi-bit errors using embedded erasure coding **2015**,		5
213	A GPU-accelerated cortical neural network model for visually guided robot navigation. *Neural Networks*, **2015**, 72, 75-87	9.1	22
212	Run-DMC: Runtime dynamic heterogeneous multicore performance and power estimation for energy efficiency **2015**,		10
211	Memory-aware cooperative CPU-GPU DVFS governor for mobile games **2015**,		5
210	Self-aware Cyber-Physical Systems-on-Chip **2015**,		11
209	NSF expedition on variability-aware software: Recent results and contributions. *IT - Information Technology*, **2015**, 57, 181-198	0.4	8

208	CARLsim 3: A user-friendly and highly optimized library for the creation of neurobiologically detailed spiking neural networks **2015**,		29
207	. *IEEE Embedded Systems Letters*, **2015**, 7, 37-40	1	4
206	Exploiting Partially-Forgetful Memories for Approximate Computing. *IEEE Embedded Systems Letters*, **2015**, 7, 19-22	1	47
205	DPCS. *Transactions on Architecture and Code Optimization*, **2015**, 12, 1-26	1.3	9
204	Multi-Layer Memory Resiliency **2014**,		10
203	GPGPU accelerated simulation and parameter tuning for neuromorphic applications **2014**,		3
202	Multicopy Cache. *Transactions on Embedded Computing Systems*, **2014**, 13, 1-27	1.8	2
201	Sense-making from Distributed and Mobile Sensing Data **2014**,		5
200	An efficient automated parameter tuning framework for spiking neural networks. *Frontiers in Neuroscience*, **2014**, 8, 10	5.1	39
199	NoC-based fault-tolerant cache design in chip multiprocessors. *Transactions on Embedded Computing Systems*, **2014**, 13, 1-26	1.8	1
198	Power / Capacity Scaling **2014**,		18
197	Quality-aware mobile graphics workload characterization for energy-efficient DVFS design **2014**,		13
196	Mechanisms underlying the basal forebrain enhancement of top-down and bottom-up attention. *European Journal of Neuroscience*, **2014**, 39, 852-65	3.5	18
195	Minimal sparse observability of complex networks: Application to MPSoC sensor placement and run-time thermal estimation & tracking **2014**,		3
194	FPGA emulation and prototyping of a cyberphysical-system-on-chip (CPSoC) **2014**,		7
193	Minimal sparse observability of complex networks: Application to MPSoC sensor placement and run-time thermal estimation & tracking **2014**,		2
192	Reliable on-chip systems in the nano-era **2013**,		111
191	REMEDIATE: A scalable fault-tolerant architecture for low-power NUCA cache in tiled CMPs **2013**,		7

#	Title	IF	Cit.
190	**2013**,		14
189	Variability-aware memory management for nanoscale computing **2013**,		3
188	Underdesigned and Opportunistic Computing in Presence of Hardware Variability. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 8-23	2.5	88
187	Biologically plausible models of homeostasis and STDP: Stability and learning in spiking neural networks **2013**,		19
186	VAWOM **2013**,		6
185	Design space exploration and parameter tuning for neuromorphic applications **2013**,		1
184	A large-scale neural network model of the influence of neuromodulatory levels on working memory and behavior. *Frontiers in Computational Neuroscience*, **2013**, 7, 133	3.5	15
183	Guest Editorial Special Section on Memory Architectures and Organization. *IEEE Embedded Systems Letters*, **2012**, 4, 81-81	1	
182	PTL: PCM Translation Layer **2012**,		11
181	Spiking neuron model of basal forebrain enhancement of visual attention **2012**,		3
180	Integrated Kernel Partitioning and Scheduling for Coarse-Grained Reconfigurable Arrays. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 1803-1816	2.5	15
179	Resilient dependable cyber-physical systems: a middleware perspective. *Journal of Internet Services and Applications*, **2012**, 3, 41-49	2.6	25
178	xTune. *Transactions on Embedded Computing Systems*, **2012**, 11, 1-23	1.8	15
177	Combining code reordering and cache configuration. *Transactions on Embedded Computing Systems*, **2012**, 11, 1-20	1.8	1
176	Error-Aware Algorithm/Architecture Coexploration for Video Over Wireless Applications. *Transactions on Embedded Computing Systems*, **2012**, 11S, 1-23	1.8	4
175	EAVE. *Transactions on Embedded Computing Systems*, **2012**, 11, 1-28	1.8	1
174	HaVOC **2012**,		17
173	Cross-layer virtual observers for embedded multiprocessor system-on-chip (MPSoC) **2012**,		10

172	ViPZonE **2012**,		13
171	A novel NoC-based design for fault-tolerance of last-level caches in CMPs **2012**,		5
170	AVid: Annotation driven video decoding for hybrid memories **2012**,		6
169	A Multi-Granularity Power Modeling Methodology for Embedded Processors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 668-681	2.6	16
168	An efficient simulation environment for modeling large-scale cortical processing. *Frontiers in Neuroinformatics*, **2011**, 5, 19	3.9	45
167	FFT-cache **2011**,		17
166	Neuromorphic modeling abstractions and simulation of large-scale cortical networks **2011**,		2
165	Slack-aware scheduling on Coarse Grained Reconfigurable Arrays **2011**,		5
164	DynaPoMP **2011**,		2
163	A Formal Methodology for Compositional Cross-Layer Optimization. *Lecture Notes in Computer Science*, **2011**, 207-222	0.9	
162	Towards reverse engineering the brain: Modeling abstractions and simulation frameworks **2010**,		3
161	ExCCel: Exploration of complementary cells for efficient DPA attack resistivity **2010**,		4
160	Bandwidth Management in Application Mapping for Dynamically Reconfigurable Architectures. *ACM Transactions on Reconfigurable Technology and Systems*, **2010**, 3, 1-30	2.7	
159	Partitioning techniques for partially protected caches in resource-constrained embedded systems. *ACM Transactions on Design Automation of Electronic Systems*, **2010**, 15, 1-30	1.5	4
158	CAPPS: A Framework for Power-Performance Tradeoffs in Bus-Matrix-Based On-Chip Communication Architecture Synthesis. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 209-221	2.6	6
157	Evaluating Carbon Nanotube Global Interconnects for Chip Multiprocessor Applications. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 1376-1380	2.6	11
156	E 2010,		26
155	PoliMakE **2010**,		7

154	RELOCATE: Register File Local Access Pattern Redistribution Mechanism for Power and Thermal Management in Out-of-Order Embedded Processor. *Lecture Notes in Computer Science*, **2010**, 216-231	0.9	7
153	Routing-Aware Application Mapping Considering Steiner Points for Coarse-Grained Reconfigurable Architecture. *Lecture Notes in Computer Science*, **2010**, 231-243	0.9	9
152	Electronic system-level design and high-level synthesis **2009**, 235-297		2
151	TRAM: A tool for Temperature and Reliability Aware Memory Design **2009**,		2
150	Computing spike-based convolutions on GPUs **2009**,		6
149	Live demonstration: Computing spike-based convolutions on GPUs **2009**,		2
148	Hybrid-compiled simulation. *Transactions on Embedded Computing Systems*, **2009**, 8, 1-27	1.8	10
147	System-level PVT variation-aware power exploration of on-chip communication architectures. *ACM Transactions on Design Automation of Electronic Systems*, **2009**, 14, 1-25	1.5	1
146	Brain Derived Vision Algorithm on High Performance Architectures. *International Journal of Parallel Programming*, **2009**, 37, 345-369	1.5	3
145	CODES+ISSS 2007 guest editorsIntroduction. *Design Automation for Embedded Systems*, **2009**, 13, 51-52	0.6	
144	A configurable simulation environment for the efficient simulation of large-scale spiking neural networks on graphics processors. *Neural Networks*, **2009**, 22, 791-800	9.1	141
143	Exploring Carbon Nanotube Bundle Global Interconnects for Chip Multiprocessor Applications **2009**,		2
142	Cross-Abstraction Functional Verification and Performance Analysis of Chip Multiprocessor Designs. *IEEE Transactions on Industrial Informatics*, **2009**, 5, 241-256	11.9	4
141	Efficient simulation of large-scale Spiking Neural Networks using CUDA graphics processors **2009**,		37
140	A Conservative Approximation Method for the Verification of Preemptive Scheduling Using Timed Automata **2009**,		6
139	Partially Protected Caches to Reduce Failures Due to Soft Errors in Multimedia Applications. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2009**, 17, 1343-1347	2.6	10
138	On chip Communication-Architecture Based Thermal Management for SoCs **2009**,		1
137	Compiler-in-the-Loop Design Space Exploration Framework for Energy Reduction in Horizontally Partitioned Cache Architectures. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2009**, 28, 461-465	2.5	2

136	Energy-aware cosynthesis of real-time multimedia applications on MPSoCs using heterogeneous scheduling policies. *Transactions on Embedded Computing Systems*, **2008**, 7, 1-19	1.8	16
135	Register File Power Reduction Using Bypass Sensitive Compiler. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2008**, 27, 1155-1159	2.5	14
134	System level performance analysis of carbon nanotube global interconnects for emerging chip multiprocessors **2008**,		6
133	Memory-aware NoC Exploration and Design **2008**,		7
132	Incorporating PVT Variations in System-Level Power Exploration of On-Chip Communication Architectures **2008**,		2
131	ORB: An on-chip optical ring bus communication architecture for multi-processor systems-on-chip **2008**,		29
130	EXPRESSION: A Language for Architecture Exploration Through Compiler/Simulator Retargetability **2008**, 31-45		6
129	Cross-layer co-exploration of exploiting error resilience for video over wireless applications **2008**,		5
128	Real-time analysis of resource-constrained distributed systems by simulation-guided model checking. *ACM SIGBED Review*, **2008**, 5, 1-2	1.3	
127	Specification-driven directed test generation for validation of pipelined processors. *ACM Transactions on Design Automation of Electronic Systems*, **2008**, 13, 1-36	1.5	23
126	Constraint refinement for online verifiable cross-layer system adaptation **2008**,		4
125	Mitigating the impact of hardware defects on multimedia applications **2008**,		12
124	Fast exploration of bus-based communication architectures at the CCATB abstraction. *Transactions on Embedded Computing Systems*, **2008**, 7, 1-32	1.8	265
123	Constraint Refinement for Online Verifiable Cross-Layer System Adaptation **2008**,		4
122	Evaluating memory architectures for media applications on Coarse-grained Reconfigurable Architectures. *International Journal of Embedded Systems*, **2008**, 3, 119	0.5	2
121	Trends in Emerging On-Chip Interconnect Technologies. *IPSJ Transactions on System LSI Design Methodology*, **2008**, 1, 2-17	0.2	26
120	Introduction to Architecture Description Languages **2008**, 1-12		1
119	Using FORAY Models to Enable MPSoC Memory Optimizations. *International Journal of Parallel Programming*, **2008**, 36, 93-113	1.5	

118	Compiler driven data layout optimization for regular/irregular array access patterns **2008**,		8
117	Compiler driven data layout optimization for regular/irregular array access patterns. *ACM SIGPLAN Notices*, **2008**, 43, 41-50	0.2	1
116	Models for Power and Thermal Estimation **2008**, 143-184		
115	Basic Concepts of Bus-Based Communication Architectures **2008**, 17-41		1
114	Models for Performance Exploration **2008**, 101-142		
113	Verification and Security Issues in On-Chip Communication Architecture Design **2008**, 367-402		
112	Emerging On-Chip Interconnect Technologies **2008**, 473-507		
111	EXPRESSION **2008**, 133-161		
110	Methodology for multi-granularity embedded processor power model generation for an ESL design flow **2008**,		6
109	On-Chip Communication Architecture Standards **2008**, 43-100		1
108	Synthesis of On-Chip Communication Architectures **2008**, 185-252		18
107	Encoding Techniques for On-Chip Communication Architectures **2008**, 253-300		6
106	Networks-On-Chip **2008**, 439-471		2
105	Data Partitioning Techniques for Partially Protected Caches to Reduce Soft Error Induced Failures. *International Federation for Information Processing*, **2008**, 213-225		1
104	Error-Exploiting Video Encoder to Extend Energy/QoS Tradeoffs for Mobile Embedded Systems. *International Federation for Information Processing*, **2008**, 23-34		3
103	STEFAL: A System Level Temperature- and Floorplan-Aware Leakage Power Estimator for SoCs **2007**,		6
102	DYNAMO: A Cross-Layer Framework for End-to-End QoS and Energy Optimization in Mobile Handheld Devices. *IEEE Journal on Selected Areas in Communications*, **2007**, 25, 722-737	14.2	39
101	Quality-Based Backlight Optimization for Video Playback on Handheld Devices. *Advances in Multimedia*, **2007**, 2007, 1-10	0.9	29

100	Enabling heterogeneous cycle-based and event-driven simulation in a design flow integrated using the SPIRIT consortium specifications. *Design Automation for Embedded Systems*, **2007**, 11, 119-140	0.6	2
99	DRDU. *ACM Transactions on Design Automation of Electronic Systems*, **2007**, 12, 15	1.5	34
98	Selective bandwidth and resource management in scheduling for dynamically reconfigurable architectures. *Proceedings - Design Automation Conference*, **2007**,		4
97	Performance estimation of distributed real-time embedded systems by discrete event simulations **2007**,		10
96	**2007**,		2
95	System level power estimation methodology with H.264 decoder prediction IP case study **2007**,		8
94	Accelerating Brain Circuit Simulations of Object Recognition with CELL Processors **2007**,		2
93	Software controlled memory layout reorganization for irregular array access patterns **2007**,		8
92	Data Reuse Driven Memory and Network-On-Chip Co-Synthesis **2007**, 299-312		1
91	Compiler-Aided Design of Embedded Computers **2007**, 3-1-3-36		
90	A Probabilistic Formal Analysis Approach to Cross Layer Optimization in Distributed Embedded Systems. *Lecture Notes in Computer Science*, **2007**, 285-300	0.9	14
89	Combining Formal Verification with Observed System Execution Behavior to Tune System Parameters. *Lecture Notes in Computer Science*, **2007**, 257-273	0.9	7
88	Architecture Description Languages **2007**, 59-76		2
87	Modeling of Software-Hardware Complexes **2007**, 423-425		
86	PARLGRAN **2006**,		12
85	Floorplan driven leakage power aware IP-based SoC design space exploration **2006**,		3
84	Formal performance evaluation of AMBA-based system-on-chip designs **2006**,		8
83	Architecture description language (ADL)-driven software toolkit generation for architectural exploration of programmable SOCs. *ACM Transactions on Design Automation of Electronic Systems*, **2006**, 11, 626-658	1.5	13

No	Title		Cites
82	Constraint-driven bus matrix synthesis for MPSoC **2006**,		13
81	Data reuse driven energy-aware MPSoC co-synthesis of memory and communication architecture for streaming applications **2006**,		9
80	Multiprocessor system-on-chip data reuse analysis for exploring customized memory hierarchies **2006**,		24
79	Memory optimal single appearance schedule with dynamic loop count for synchronous dataflow graphs **2006**,		12
78	Design space exploration of real-time multi-media MPSoCs with heterogeneous scheduling policies **2006**,		15
77	Compilation framework for code size reduction using reduced bit-width ISAs (rISAs). *ACM Transactions on Design Automation of Electronic Systems*, **2006**, 11, 123-146	1.5	9
76	A retargetable framework for instruction-set architecture simulation. *Transactions on Embedded Computing Systems*, **2006**, 5, 431-452	1.8	11
75	System-level power-performance trade-offs in bus matrix communication architecture synthesis **2006**,		21
74	Video Stream Annotations for Energy Trade-offs in Multimedia Applications **2006**,		1
73	Annotation Based Multimedia Streaming Over Wireless Networks **2006**,		3
72	Bypass aware instruction scheduling for register file power reduction. *ACM SIGPLAN Notices*, **2006**, 41, 173-181	0.2	9
71	Bypass aware instruction scheduling for register file power reduction **2006**,		25
70	PBPAIR. *Mobile Computing and Communications Review*, **2006**, 10, 58-69		14
69	Mitigating soft error failures for multimedia applications by selective data protection **2006**,		38
68	Domain-Specific Modeling of Power Aware Distributed Real-Time Embedded Systems. *Lecture Notes in Computer Science*, **2006**, 59-68	0.9	2
67	A methodology for validation of microprocessors using symbolic simulation. *International Journal of Embedded Systems*, **2005**, 1, 14	0.5	1
66	Quality Adapted Backlight Scaling (QABS) for Video Streaming to Mobile Handheld Devices. *Lecture Notes in Computer Science*, **2005**, 662-671	0.9	6
65	A first look at the interplay of code reordering and configurable caches **2005**,		6

64	Physically-aware HW-SW partitioning for reconfigurable architectures with partial dynamic reconfiguration **2005**,		42
63	Floorplan-aware automated synthesis of bus-based communication architectures **2005**,		29
62	Automated throughput-driven synthesis of bus-based communication architectures **2005**,		2
61	Shift buffering technique for automatic code synthesis from synchronous dataflow graphs **2005**,		3
60	Fast configurable-cache tuning with a unified second-level cache **2005**,		18
59	Aggregating processor free time for energy reduction **2005**,		9
58	Compilation techniques for energy reduction in horizontally partitioned cache architectures **2005**,		31
57	Single appearance schedule with dynamic loop count for minimum data buffer from synchronous dataflow graphs **2005**,		8
56	Memory Systems and Compiler Support for MPSoC Architectures **2005**, 251-281		9
55	Energy-Aware Adaptations for End-to-End Videostreaming to Mobile Handheld Devices **2004**, 255-273		0
54	Introduction of local memory elements in instruction set extensions **2004**,		22
53	Extending the transaction level modeling approach for fast communication architecture exploration **2004**,		24
52	Modeling and validation of pipeline specifications. *Transactions on Embedded Computing Systems*, **2004**, 3, 114-139	1.8	15
51	Processor-memory coexploration using an architecture description language. *Transactions on Embedded Computing Systems*, **2004**, 3, 140-162	1.8	7
50	. *IEEE Design and Test of Computers*, **2004**, 21, 122-131		9
49	Fast exploration of bus-based on-chip communication architectures **2004**,		38
48	Dynamic backlight adaptation for low-power handheld devices. *IEEE Design and Test of Computers*, **2004**, 21, 398-405		29
47	Operation tables for scheduling in the presence of incomplete bypassing **2004**,		12

46	Analytical models for leakage power estimation of memory array structures **2004**,		12
45	Proxy-based task partitioning of watermarking algorithms for reducing energy consumption in mobile devices **2004**,		3
44	Efficient search space exploration for HW-SW partitioning **2004**,		21
43	Interconnect-Aware Mapping of Applications to Coarse-Grain Reconfigurable Architectures. *Lecture Notes in Computer Science*, **2004**, 891-899	0.9	8
42	Integrated power management for video streaming to mobile handheld devices **2003**,		41
41	Instruction set compiled simulation **2003**,		39
40	Reducing code size for heterogeneous-connectivity-based VLIW DSPs through synthesis of instruction set extensions **2003**,		2
39	Access pattern-based memory and connectivity architecture exploration. *Transactions on Embedded Computing Systems*, **2003**, 2, 33-73	1.8	4
38	An efficient retargetable framework for instruction-set simulation **2003**,		19
37	Towards Automatic Validation of Dynamic Behavior in Pipelined Processor Specifications. *Design Automation for Embedded Systems*, **2003**, 8, 249-265	0.6	5
36	Dynamic common sub-expression elimination during scheduling in high-level synthesis **2002**,		7
35	Efficient instruction encoding for automatic instruction set design of configurable ASIPs. *IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers*, **2002**,		15
34	Coordinated transformations for high-level synthesis of high performance microprocessor blocks. *Proceedings - Design Automation Conference*, **2002**,		5
33	Modeling and Verification of Pipelined Embedded Processors in the Presence of Hazards and Exceptions. *IFIP Advances in Information and Communication Technology*, **2002**, 81-90	0.5	4
32	V-SAT: A visual specification and analysis tool for system-on-chip exploration. *Journal of Systems Architecture*, **2001**, 47, 263-275	5.5	1
31	New directions in compiler technology for embedded systems (embedded tutorial) **2001**,		4
30	Low power address encoding using self-organizing lists **2001**,		8
29	APEX **2001**,		12

28	Functional abstraction driven design space exploration of heterogeneous programmable architectures **2001**,		25
27	Speculation techniques for high level synthesis of control intensive designs **2001**,		16
26	Customizing Software Toolkits for Embedded Systems-on-Chip. *IFIP Advances in Information and Communication Technology*, **2001**, 87-97	0.5	
25	Memory aware compilation through accurate timing extraction **2000**,		24
24	EXPRESSION **1999**,		162
23	Memory Issues in Embedded Systems-on-Chip **1999**,		94
22	Copy Elimination for Parallelizing Compilers. *Lecture Notes in Computer Science*, **1999**, 275-289	0.9	
21	Memory size estimation for multimedia applications **1998**,		8
20	Optimal register assignment to loops for embedded code generation. *ACM Transactions on Design Automation of Electronic Systems*, **1996**, 1, 251-279	1.5	21
19	A hypergraph-based model for port allocation on multiple-register-file VLIW architectures. *International Journal of Parallel Programming*, **1995**, 23, 499-513	1.5	3
18	A comprehensive estimation technique for high-level synthesis **1995**,		8
17	Minimization of memory traffic in high-level synthesis **1994**,		6
16	**1994**,		3
15	High-level synthesis of scalable architectures for IIR filters using multichip modules **1993**,		2
14	Partitioned register files for VLIWs. *ACM SIGMICRO Newsletter*, **1992**, 23, 292-300		15
13	Constraint-driven bus matrix synthesis for MPSoC		8
12	Probability based power aware error resilient coding		1
11	A cross-layer approach for power-performance optimization in distributed mobile systems		25

10	PARLGRAN: parallelism granularity selection for scheduling task chains on dynamically reconfigurable architectures	2
9	Energy efficient code generation exploiting reduced bit-width instruction set architectures (rISA)	1
8	Interface synthesis using memory mapping for an FPGA platform	8
7	Generic pipelined processor modeling and high performance cycle-accurate simulator generation	5
6		32
5	FORAY-GEN: automatic generation of affine functions for memory optimizations	11
4	PBExplore: a framework for compiler-in-the-loop exploration of partial bypassing in embedded processors	7
3	Sleep Tracking of a Commercially Available Smart Ring and Smartwatch Against Medical-Grade Actigraphy in Everyday Settings: Instrument Validation Study (Preprint)	1
2	Sparse coding and dimensionality reduction in cortex	2
1	Exploring Energy Efficient Architectures for RLWE Lattice-Based Cryptography. *Journal of Signal Processing Systems*,1	1.4