Nikil Dutt

List of Publications by Citations

333 papers	3,918 citations	29 h-index	47 g-index
394 ext. papers	4,968 ext. citations	2.5 avg, IF	5.63 L-index

#	Paper	IF	Citations
333	Fast exploration of bus-based communication architectures at the CCATB abstraction. *Transactions on Embedded Computing Systems*, **2008**, 7, 1-32	1.8	265
332	EXPRESSION **1999**,		162
331	A configurable simulation environment for the efficient simulation of large-scale spiking neural networks on graphics processors. *Neural Networks*, **2009**, 22, 791-800	9.1	141
330	Reliable on-chip systems in the nano-era **2013**,		111
329	Memory Issues in Embedded Systems-on-Chip **1999**,		94
328	Underdesigned and Opportunistic Computing in Presence of Hardware Variability. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 8-23	2.5	88
327	HiCH. *Transactions on Embedded Computing Systems*, **2017**, 16, 1-20	1.8	80
326	Post-Quantum Lattice-Based Cryptography Implementations. *ACM Computing Surveys*, **2019**, 51, 1-41	13.4	63
325	SPARTA **2016**,		49
324	Toward Smart Embedded Systems. *Transactions on Embedded Computing Systems*, **2016**, 15, 1-27	1.8	49
323	Exploiting Partially-Forgetful Memories for Approximate Computing. *IEEE Embedded Systems Letters*, **2015**, 7, 19-22	1	47
322	An efficient simulation environment for modeling large-scale cortical processing. *Frontiers in Neuroinformatics*, **2011**, 5, 19	3.9	45
321	Physically-aware HW-SW partitioning for reconfigurable architectures with partial dynamic reconfiguration **2005**,		42
320	Integrated power management for video streaming to mobile handheld devices **2003**,		41
319	An efficient automated parameter tuning framework for spiking neural networks. *Frontiers in Neuroscience*, **2014**, 8, 10	5.1	39
318	DYNAMO: A Cross-Layer Framework for End-to-End QoS and Energy Optimization in Mobile Handheld Devices. *IEEE Journal on Selected Areas in Communications*, **2007**, 25, 722-737	14.2	39
317	Instruction set compiled simulation **2003**,		39

316	Fast exploration of bus-based on-chip communication architectures **2004**,		38
315	Mitigating soft error failures for multimedia applications by selective data protection **2006**,		38
314	Efficient simulation of large-scale Spiking Neural Networks using CUDA graphics processors **2009**,		37
313	CARLsim 4: An Open Source Library for Large Scale, Biologically Detailed Spiking Neural Network Simulation using Heterogeneous Clusters **2018**,		37
312	Unsupervised heart-rate estimation in wearables with Liquid states and a probabilistic readout. *Neural Networks*, **2018**, 99, 134-147	9.1	36
311	DRDU. *ACM Transactions on Design Automation of Electronic Systems*, **2007**, 12, 15	1.5	34
310			32
309	Compilation techniques for energy reduction in horizontally partitioned cache architectures **2005**,		31
308	Self-awareness in remote health monitoring systems using wearable electronics **2017**,		29
307	Neural correlates of sparse coding and dimensionality reduction. *PLoS Computational Biology*, **2019**, 15, e1006908	5	29
306	CARLsim 3: A user-friendly and highly optimized library for the creation of neurobiologically detailed spiking neural networks **2015**,		29
305	ORB: An on-chip optical ring bus communication architecture for multi-processor systems-on-chip **2008**,		29
304	Quality-Based Backlight Optimization for Video Playback on Handheld Devices. *Advances in Multimedia*, **2007**, 2007, 1-10	0.9	29
303	Dynamic backlight adaptation for low-power handheld devices. *IEEE Design and Test of Computers*, **2004**, 21, 398-405		29
302	Floorplan-aware automated synthesis of bus-based communication architectures **2005**,		29
301	E 2010,		26
300	Trends in Emerging On-Chip Interconnect Technologies. *IPSJ Transactions on System LSI Design Methodology*, **2008**, 1, 2-17	0.2	26
299	Resilient dependable cyber-physical systems: a middleware perspective. *Journal of Internet Services and Applications*, **2012**, 3, 41-49	2.6	25

298	A cross-layer approach for power-performance optimization in distributed mobile systems		25
297	Functional abstraction driven design space exploration of heterogeneous programmable architectures **2001**,		25
296	Bypass aware instruction scheduling for register file power reduction **2006**,		25
295	Sleep Tracking of a Commercially Available Smart Ring and Smartwatch Against Medical-Grade Actigraphy in Everyday Settings: Instrument Validation Study. *JMIR MHealth and UHealth*, **2020**, 8, e20465	5.5	25
294	A Real-time PPG Quality Assessment Approach for Healthcare Internet-of-Things. *Procedia Computer Science*, **2019**, 151, 551-558	1.6	24
293	Multiprocessor system-on-chip data reuse analysis for exploring customized memory hierarchies **2006**,		24
292	Extending the transaction level modeling approach for fast communication architecture exploration **2004**,		24
291	Memory aware compilation through accurate timing extraction **2000**,		24
290	Specification-driven directed test generation for validation of pipelined processors. *ACM Transactions on Design Automation of Electronic Systems*, **2008**, 13, 1-36	1.5	23
289	A GPU-accelerated cortical neural network model for visually guided robot navigation. *Neural Networks*, **2015**, 72, 75-87	9.1	22
288	Introduction of local memory elements in instruction set extensions **2004**,		22
287	Optimal register assignment to loops for embedded code generation. *ACM Transactions on Design Automation of Electronic Systems*, **1996**, 1, 251-279	1.5	21
286	System-level power-performance trade-offs in bus matrix communication architecture synthesis **2006**,		21
285	Efficient search space exploration for HW-SW partitioning **2004**,		21
284	SPECTR **2018**,		20
283	Self-Awareness in Systems on Chip□A Survey. *IEEE Design and Test*, **2017**, 34, 8-26	1.4	20
282	. *IEEE Access*, **2019**, 7, 93433-93447	3.5	19
281	Biologically plausible models of homeostasis and STDP: Stability and learning in spiking neural networks **2013**,		19

280	An efficient retargetable framework for instruction-set simulation **2003**,		19
279	Power / Capacity Scaling **2014**,		18
278	Mechanisms underlying the basal forebrain enhancement of top-down and bottom-up attention. *European Journal of Neuroscience*, **2014**, 39, 852-65	3.5	18
277	Fast configurable-cache tuning with a unified second-level cache **2005**,		18
276	Synthesis of On-Chip Communication Architectures **2008**, 185-252		18
275	FFT-cache **2011**,		17
274	HaVOC **2012**,		17
273	A Framework to Explore Workload-Specific Performance and Lifetime Trade-offs in Neuromorphic Computing. *IEEE Computer Architecture Letters*, **2019**, 18, 149-152	1.8	17
272	Neural and Synaptic Array Transceiver: A Brain-Inspired Computing Framework for Embedded Learning. *Frontiers in Neuroscience*, **2018**, 12, 583	5.1	17
271	Thermal-Aware Task Mapping on Dynamically Reconfigurable Network-on-Chip Based Multiprocessor System-on-Chip. *IEEE Transactions on Computers*, **2018**, 67, 1818-1834	2.5	16
270	A Multi-Granularity Power Modeling Methodology for Embedded Processors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 668-681	2.6	16
269	Energy-aware cosynthesis of real-time multimedia applications on MPSoCs using heterogeneous scheduling policies. *Transactions on Embedded Computing Systems*, **2008**, 7, 1-19	1.8	16
268	Speculation techniques for high level synthesis of control intensive designs **2001**,		16
267	Integrated Kernel Partitioning and Scheduling for Coarse-Grained Reconfigurable Arrays. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 1803-1816	2.5	15
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263	Modeling and validation of pipeline specifications. *Transactions on Embedded Computing Systems*, **2004**, 3, 114-139	1.8	15

262	Efficient instruction encoding for automatic instruction set design of configurable ASIPs. *IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers*, **2002**,		15
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252	Constraint-driven bus matrix synthesis for MPSoC **2006**,		13
251	QuARK: Quality-configurable approximate STT-MRAM cache by fine-grained tuning of reliability-energy knobs **2017**,		12
250	Mitigating the impact of hardware defects on multimedia applications **2008**,		12
249	PARLGRAN **2006**,		12
248	Memory optimal single appearance schedule with dynamic loop count for synchronous dataflow graphs **2006**,		12
247	Operation tables for scheduling in the presence of incomplete bypassing **2004**,		12
246	Analytical models for leakage power estimation of memory array structures **2004**,		12
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244	Self-aware Cyber-Physical Systems-on-Chip **2015**,		11
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241	A retargetable framework for instruction-set architecture simulation. *Transactions on Embedded Computing Systems*, **2006**, 5, 431-452	1.8	11
240	FORAY-GEN: automatic generation of affine functions for memory optimizations		11
239	HiCAP **2016**,		11
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229	Goal-Driven Autonomy for Efficient On-chip Resource Management: Transforming Objectives to Goals **2019**,		9
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215	Trends, challenges and needs for lattice-based cryptography implementations **2017**,		8
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213	NSF expedition on variability-aware software: Recent results and contributions. *IT - Information Technology*, **2015**, 57, 181-198	0.4	8
212	Formal performance evaluation of AMBA-based system-on-chip designs **2006**,		8
211	Constraint-driven bus matrix synthesis for MPSoC		8
210	System level power estimation methodology with H.264 decoder prediction IP case study **2007**,		8
209	Interface synthesis using memory mapping for an FPGA platform		8

208	Low power address encoding using self-organizing lists **2001**,		8
207	Single appearance schedule with dynamic loop count for minimum data buffer from synchronous dataflow graphs **2005**,		8
206	Software controlled memory layout reorganization for irregular array access patterns **2007**,		8
205	Compiler driven data layout optimization for regular/irregular array access patterns **2008**,		8
204	A comprehensive estimation technique for high-level synthesis **1995**,		8
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202	SOSA **2019**,		8
201	Interconnect-Aware Mapping of Applications to Coarse-Grain Reconfigurable Architectures. *Lecture Notes in Computer Science*, **2004**, 891-899	0.9	8
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196	FPGA emulation and prototyping of a cyberphysical-system-on-chip (CPSoC) **2014**,		7
195	Memory-aware NoC Exploration and Design **2008**,		7
194	Processor-memory coexploration using an architecture description language. *Transactions on Embedded Computing Systems*, **2004**, 3, 140-162	1.8	7
193	PBExplore: a framework for compiler-in-the-loop exploration of partial bypassing in embedded processors		7
192	Dynamic common sub-expression elimination during scheduling in high-level synthesis **2002**,		7
191	PoliMakE **2010**,		7

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188	An Efficient and Robust Deep Learning Method with 1-D Octave Convolution to Extract Fetal Electrocardiogram. *Sensors*, **2020**, 20,	3.8	7
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186	Long-Term IoT-Based Maternal Monitoring: System Design and Evaluation. *Sensors*, **2021**, 21,	3.8	7
185	An Edge-Assisted and Smart System for Real-Time Pain Monitoring **2019**,		7
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183	Small Memory Footprint Neural Network Accelerators **2019**,		6
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177	Computing spike-based convolutions on GPUs **2009**,		6
176	AVid: Annotation driven video decoding for hybrid memories **2012**,		6
175	A Conservative Approximation Method for the Verification of Preemptive Scheduling Using Timed Automata **2009**,		6
174	System level performance analysis of carbon nanotube global interconnects for emerging chip multiprocessors **2008**,		6
173	EXPRESSION: A Language for Architecture Exploration Through Compiler/Simulator Retargetability **2008**, 31-45		6

172	STEFAL: A System Level Temperature- and Floorplan-Aware Leakage Power Estimator for SoCs **2007**,		6
171	Quality Adapted Backlight Scaling (QABS) for Video Streaming to Mobile Handheld Devices. *Lecture Notes in Computer Science*, **2005**, 662-671	0.9	6
170	A first look at the interplay of code reordering and configurable caches **2005**,		6
169	Minimization of memory traffic in high-level synthesis **1994**,		6
168	Co-Cap **2016**,		6
167	Methodology for multi-granularity embedded processor power model generation for an ESL design flow **2008**,		6
166	Encoding Techniques for On-Chip Communication Architectures **2008**, 253-300		6
165	Design methodologies for enabling self-awareness in autonomous systems **2018**,		6
164	Protecting caches against multi-bit errors using embedded erasure coding **2015**,		5
163	HDGM: Hierarchical Dynamic Goal Management for Many-Core Resource Allocation. *IEEE Embedded Systems Letters*, **2018**, 10, 61-64	1	5
162	Automatic management of Software Programmable Memories in Many-core Architectures. *IET Computers and Digital Techniques*, **2016**, 10, 288-298	0.9	5
161	SPMPool. *Transactions on Embedded Computing Systems*, **2016**, 16, 1-27	1.8	5
160	Conquering MPSoC complexity with principles of a self-aware information processing factory **2016**,		5
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158	Sense-making from Distributed and Mobile Sensing Data **2014**,		5
157	Memory-aware cooperative CPU-GPU DVFS governor for mobile games **2015**,		5
156	Slack-aware scheduling on Coarse Grained Reconfigurable Arrays **2011**,		5
155	A novel NoC-based design for fault-tolerance of last-level caches in CMPs **2012**,		5

154	Cross-layer co-exploration of exploiting error resilience for video over wireless applications **2008**,		5
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117	GPGPU accelerated simulation and parameter tuning for neuromorphic applications **2014**,		3
116	Variability-aware memory management for nanoscale computing **2013**,		3
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108	Proxy-based task partitioning of watermarking algorithms for reducing energy consumption in mobile devices **2004**,		3
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89	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 4385-4398	2.5	2
88	Multicopy Cache. *Transactions on Embedded Computing Systems*, **2014**, 13, 1-27	1.8	2
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85	TRAM: A tool for Temperature and Reliability Aware Memory Design **2009**,		2
84	Live demonstration: Computing spike-based convolutions on GPUs **2009**,		2
83	Exploring Carbon Nanotube Bundle Global Interconnects for Chip Multiprocessor Applications **2009** ,		2

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81	DynaPoMP **2011**,		2
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74	PARLGRAN: parallelism granularity selection for scheduling task chains on dynamically reconfigurable architectures		2
73	Reducing code size for heterogeneous-connectivity-based VLIW DSPs through synthesis of instruction set extensions **2003**,		2
72	Automated throughput-driven synthesis of bus-based communication architectures **2005**,		2
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