Hongwu Jiang

List of Publications by Year
in descending order

16 papers	489 citations	1163117 8 h-index	1588992 8 g-index
16 all docs	16 docs citations	16 times ranked	323 citing authors

#	Article	IF	Citations
1	Two-Way Transpose Multibit 6T SRAM Computing-in-Memory Macro for Inference-Training AI Edge Chips. IEEE Journal of Solid-State Circuits, 2022, 57, 609-624.	5.4	18
2	Analog-to-Digital Converter Design Exploration for Compute-in-Memory Accelerators. IEEE Design and Test, 2022, 39, 48-55.	1.2	16
3	Achieving High In Situ Training Accuracy and Energy Efficiency with Analog Non-Volatile Synaptic Devices. ACM Transactions on Design Automation of Electronic Systems, 2022, 27, 1-19.	2.6	0
4	A 40-nm MLC-RRAM Compute-in-Memory Macro With Sparsity Control, On-Chip Write-Verify, and Temperature-Independent ADC References. IEEE Journal of Solid-State Circuits, 2022, 57, 2868-2877.	5.4	21
5	Compute-in-Memory Chips for Deep Learning: Recent Trends and Prospects. IEEE Circuits and Systems Magazine, 2021, 21, 31-56.	2.3	115
6	Exploiting Process Variations to Protect Machine Learning Inference Engine from Chip Cloning. , 2021, , .		1
7	NeuroSim Simulator for Compute-in-Memory Hardware Accelerator: Validation and Benchmark. Frontiers in Artificial Intelligence, 2021, 4, 659060.	3.4	23
8	DNN+NeuroSim V2.0: An End-to-End Benchmarking Framework for Compute-in-Memory Accelerators for On-Chip Training. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2306-2319.	2.7	96
9	Secure XOR-CIM Engine: Compute-In-Memory SRAM Architecture With Embedded XOR Encryption. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 2027-2039.	3.1	8
10	A 40nm RRAM Compute-in-Memory Macro Featuring On-Chip Write-Verify and Offset-Cancelling ADC References. , 2021, , .		0
11	A Two-way SRAM Array based Accelerator for Deep Neural Network On-chip Training. , 2020, , .		21
12	MINT: Mixed-Precision RRAM-Based IN-Memory Training Architecture. , 2020, , .		15
13	15.2 A 28nm 64Kb Inference-Training Two-Way Transpose Multibit 6T SRAM Compute-in-Memory Macro for AI Edge Chips. , 2020, , .		99
14	Overcoming Challenges for Achieving High in-situ Training Accuracy with Emerging Memories. , 2020, , .		8
15	CIMAT: A Compute-In-Memory Architecture for On-chip Training Based on Transpose SRAM Arrays. IEEE Transactions on Computers, 2020, , 1-1.	3.4	35
16	XOR-CIM. , 2020, , .		13