Deming Chen

List of Publications by Year
in descending order

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114	2,312	567281 15	677142 22
papers	citations	h-index	g-index

114	114	114	1376
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Exploring HW/SW Co-Design for Video Analysis on CPU-FPGA Heterogeneous Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1606-1619.	2.7	8
2	DML: Dynamic Partial Reconfiguration With Scalable Task Scheduling for Multi-Applications on FPGAs. IEEE Transactions on Computers, 2022, 71, 2577-2591.	3.4	5
3	HiKonv: High Throughput Quantized Convolution With Novel Bit-wise Management and Computation. , 2022, , .		4
4	Algorithm/Accelerator Co-Design and Co-Search for Edge AI. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3064-3070.	3.0	2
5	Improving the Generalization Ability of Deep Neural Networks for Cross-Domain Visual Recognition. IEEE Transactions on Cognitive and Developmental Systems, 2021, 13, 607-620.	3.8	40
6	VecQ: Minimal Loss DNN Model Compression With Vectorized Weight Quantization. IEEE Transactions on Computers, 2021, 70, 696-710.	3.4	25
7	FracBNN: Accurate and FPGA-Efficient Binary Neural Networks with Fractional Activations. , 2021, , .		49
8	TwinDNN: A Tale of Two Deep Neural Networks. , 2021, , .		0
9	Software/Hardware Co-design for Multi-modal Multi-task Learning in Autonomous Systems. , 2021, , .		10
10	Learning-Based Simultaneous Detection and Characterization of Time Delay Attack in Cyber-Physical Systems. IEEE Transactions on Smart Grid, 2021, 12, 3581-3593.	9.0	20
11	Efficient Methods for Mapping Neural Machine Translator on FPGAs. IEEE Transactions on Parallel and Distributed Systems, 2021, 32, 1866-1877.	5.6	7
12	TwinDNN: A Tale of Two Deep Neural Networks. , 2021, , .		0
13	Enabling Design Methodologies and Future Trends for Edge AI: Specialization and Codesign. IEEE Design and Test, 2021, 38, 7-26.	1.2	24
14	HELLO: improved neural network architectures and methodologies for small variant calling. BMC Bioinformatics, 2021, 22, 404.	2.6	5
15	PyLog: An Algorithm-Centric Python-Based FPGA Programming and Synthesis Flow. IEEE Transactions on Computers, 2021, , 1-1.	3.4	10
16	A Python-based High-Level Programming Flow for CPU-FPGA Heterogeneous Systems : (Invited Paper). , 2021, , .		0
17	HybridDNN: A Framework for High-Performance Hybrid DNN Accelerator Design and Implementation. , 2020, , .		39
18	EDD: Efficient Differentiable DNN Architecture and Implementation Co-search for Embedded AI Solutions. , 2020, , .		41

#	Article	IF	Citations
19	AutoDNNchip. , 2020, , .		52
20	DNNExplorer. , 2020, , .		38
21	Hybrid Quick Error Detection: Validation and Debug of SoCs Through High-Level Synthesis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1345-1358.	2.7	1
22	FPGA/DNN Co-Design. , 2019, , .		115
23	Near-Memory and In-Storage FPGA Acceleration for Emerging Cognitive Computing Workloads. , 2019, , .		5
24	Implementing neural machine translation with bi-directional GRU and attention mechanism on FPGAs using HLS. , 2019, , .		18
25	Cloud-DNN. , 2019, , .		73
26	T-DLA: An Open-source Deep Learning Accelerator for Ternarized DNN Models on Embedded FPGA. , 2019, , .		21
27	Automated Communication and Floorplan-Aware Hardware/Software Co-Design for SoC. , 2019, , .		1
28	Accelerating Sparse Deep Neural Networks on FPGAs. , 2019, , .		15
29	NAIS: Neural Architecture and Implementation Search and its Applications in Autonomous Driving. , 2019, , .		16
30	Deep Learning for Better Variant Calling for Cancer Diagnosis and Treatment. , 2018, , .		2
31	Compact Modeling to Device- and Circuit-Level Evaluation of Flexible TMD Field-Effect Transistors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 820-831.	2.7	8
32	Design Flow of Accelerating Hybrid Extremely Low Bit-Width Neural Network in Embedded FPGA. , 2018, , .		56
33	Deep Neural Network Model and FPGA Accelerator Co-Design: Opportunities and Challenges. , 2018, , .		11
34	Triangle Counting and Truss Decomposition using FPGA. , 2018, , .		13
35	DNNBuilder. , 2018, , .		224
36	Face Recognition with Hybrid Efficient Convolution Algorithms on FPGAs. , 2018, , .		26

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37	New advances of high-level synthesis for efficient and reliable hardware design. The Integration VLSI Journal, 2017, 58, 189-214.	2.1	12
38	Accurate High-level Modeling and Automated Hardware/Software Co-design for Effective SoC Design Space Exploration. , 2017, , .		25
39	Efficient GPGPU Computing with Cross-Core Resource Sharing and Core Reconfiguration. , 2017, , .		2
40	High-performance video content recognition with long-term recurrent convolutional network for FPGA. , 2017, , .		49
41	Information dispersion for trojan defense through high-level synthesis. , 2016, , .		17
42	Platform choices and design demands for IoT platforms: cost, power, and performance tradeoffs. IET Cyber-Physical Systems: Theory and Applications, 2016, 1, 70-77.	3.3	35
43	FCUDA-SoC. , 2016, , .		8
44	High Level Synthesis of Complex Applications. , 2016, , .		43
45	FCUDA-HB: Hierarchical and Scalable Bus Architecture Generation on FPGAs With the FCUDA Flow. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 2032-2045.	2.7	4
46	SoC, NoC and Hierarchical Bus Implementations of Applications on FPGAs Using the FCUDA Flow. , 2016, , .		2
47	AutoSLIDE: Automatic Source-Level Instrumentation and Debugging for HLS. , 2016, , .		9
48	Debugging and verifying SoC designs through effective cross-layer hardware-software co-simulation. , 2016, , .		18
49	FCUDA-NoC: A Scalable and Efficient Network-on-Chip Implementation for the CUDA-to-FPGA Flow. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2220-2233.	3.1	20
50	PolyPUF: Physically Secure Self-Divergence. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1053-1066.	2.7	15
51	BLESS 2: accurate, memory-efficient and fast error correction method. Bioinformatics, 2016, 32, 2369-2371.	4.1	22
52	Flexible transition metal dichalcogenide field-effect transistors: A circuit-level simulation study of delay and power under bending, process variation, and scaling. , 2016, , .		5
53	A polyhedral-based SystemC modeling and generation framework for effective low-power design space exploration. , 2015, , .		19
54	Behavioral-level IP integration in high-level synthesis. , 2015, , .		4

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55	High-level Synthesis for Low-power Design. IPSJ Transactions on System LSI Design Methodology, 2015, 8, 12-25.	0.8	22
56	A Scalable and High-Density FPGA Architecture with Multi-Level Phase Change Memory. , 2015, , .		3
57	FPGA Accelerated DNA Error Correction. , 2015, , .		10
58	JIT trace-based verification for high-level synthesis. , 2015, , .		9
59	CSL: Coordinated and scalable logic synthesis techniques for effective NBTI reduction. , 2015, , .		2
60	High-level synthesis of error detecting cores through low-cost modulo-3 shadow datapaths. , 2015, , .		15
61	Robust blind image watermarking based on chaotic mixtures. Nonlinear Dynamics, 2015, 80, 1329-1355.	5.2	31
62	Hybrid quick error detection (H-QED). , 2015, , .		13
63	New algorithms for computation acceleration for large-scale smart grids. , 2014, , .		0
64	Asymmetric Gate Schottky-Barrier Graphene Nanoribbon FETs for Low-Power Design. IEEE Transactions on Electron Devices, 2014, 61, 4000-4006.	3.0	16
65	High-Level Synthesis With Behavioral-Level Multicycle Path Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1832-1845.	2.7	9
66	Fast and effective placement and routing directed high-level synthesis for FPGAs. , 2014, , .		34
67	Analysis of System Reliability for Cache Coherence Scheme in Multi-processor. , 2014, , .		2
68	CNPUF: A Carbon Nanotube-based Physically Unclonable Function for secure low-energy hardware design. , 2014, , .		42
69	Fast large-scale optimal power flow analysis for smart grid through network reduction. , 2014, , .		3
70	Integrated CUDA-to-FPGA Synthesis with Network-on-Chip. , 2014, , .		4
71	High-level synthesis of multiple dependent CUDA kernels on FPGA. , 2013, , .		13
72	Graphene nano-ribbon field-effect transistors as future low-power devices. , 2013, , .		19

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73	Throughput-oriented kernel porting onto FPGAs. , 2013, , .		9
74	Improving polyhedral code generation for high-level synthesis. , 2013, , .		21
75	High-level synthesis with behavioral level multi-cycle path analysis. , 2013, , .		15
76	Schottky-barrier-type Graphene Nano-Ribbon Field-Effect Transistors: A study on compact modeling, process variation, and circuit performance. , 2013, , .		17
77	Efficient compilation of CUDA kernels for high-performance computing on FPGAs. Transactions on Embedded Computing Systems, 2013, 13, 1-26.	2.9	20
78	Improving high level synthesis optimization opportunity through polyhedral transformations. , 2013, , .		74
79	A real-time 3D sound localization system with miniature microphone array for virtual reality. , 2012, , .		35
80	Challenges and opportunities of ESL design automation. , 2012, , .		4
81	ESL Design Methodology. Journal of Electrical and Computer Engineering, 2012, 2012, 1-2.	0.9	0
82	Hybrid circuit-switched NOC for low cost on-chip communication. , 2012, , .		3
83	A Coarse-Grained Reconfigurable Architecture with Compilation for High Performance. International Journal of Reconfigurable Computing, 2012, 2012, 1-17.	0.2	2
84	Analysis of Digital Circuit Dynamic Behavior With Timed Ternary Decision Diagrams for Better-Than-Worst-Case Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 662-675.	2.7	4
85	Multilevel Granularity Parallelism Synthesis on FPGAs. , 2011, , .		39
86	SETmap: A soft error tolerant mapping algorithm for FPGA designs with low power. , 2011, , .		3
87	Architecture and performance evaluation of 3D CMOS-NEM FPGA. , 2011, , .		10
88	Real-Time Object Tracking System on FPGAs. , 2011, , .		29
89	A study of high-level synthesis: Promises and challenges. , 2011, , .		32
90	High level synthesis of stereo matching: Productivity, performance, and software constraints. , 2011, , .		35

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91	Variation-aware layout-driven scheduling for performance yield optimization. , 2010, , .		9
92	BDD-based circuit restructuring for reducing dynamic power. , 2010, , .		3
93	LOPASS: A Low-Power Architectural Synthesis System for FPGAs With Interconnect Estimation and Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 564-577.	3.1	40
94	A Routing Approach to Reduce Glitches in Low Power FPGAs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 235-240.	2.7	13
95	Variation-Aware Placement With Multi-Cycle Statistical Timing Analysis for FPGAs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1818-1822.	2.7	5
96	Technology Mapping and Clustering for FPGA Architectures With Dual Supply Voltages. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1709-1722.	2.7	17
97	Dynamic power estimation for deep submicron circuits with process variation. , 2010, , .		9
98	FPGA-targeted high-level binding algorithm for power and area reduction with glitch-estimation. , 2009, , .		7
99	Variation Aware Routing for Three-Dimensional FPGAs. , 2009, , .		4
100	Design and Evaluation of a Carbon Nanotube-Based Programmable Architecture. International Journal of Parallel Programming, 2009, 37, 389-416.	1.5	5
101	FastYield: Variation-aware, layout-driven simultaneous binding and module selection for performance yield optimization. , 2009, , .		13
102	A novel SoC architecture on FPGA for ultra fast face detection. , 2009, , .		30
103	Reconfigurable circuit design with nanomaterials. , 2009, , .		1
104	Blueshift: Designing processors for timing speculation from the ground up.. , 2009, , .		64
105	Workload adaptive shared memory multicore processors with reconfigurable interconnects. , 2009, , .		4
106	FCUDA: Enabling efficient compilation of CUDA kernels onto FPGAs. , 2009, , .		110
107	An Optimal Resource Binding Algorithm with Inter-Transition Switching Activities for Low Power. Journal of Low Power Electronics, 2009, 5, 454-463.	0.6	1
108	VEBoC: Variation and error-aware design for billions of devices on a chip. , 2008, , .		0

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109	3-D nFPGA: A Reconfigurable Architecture for 3-D CMOS/Nanomaterial Hybrid Digital Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2007, 54, 2489-2501.	5.4	47
110	Performance and power evaluation of a 3D CMOS/nanomaterial reconfigurable architecture. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	1
111	GlitchMap: An FPGA Technology Mapper for Low Power Considering Glitches. Proceedings - Design Automation Conference, 2007, , .	0.0	3
112	Optimality study of resource binding with multi-Vdds. Proceedings - Design Automation Conference, 2006, , .	0.0	2
113	Optimality study of resource binding with multi-Vdds. , 2006, , .		17
114	Delay optimal low-power circuit clustering for FPGAs with dual supply voltages. , 2004, , .		15