Byung-Gook Park

List of Publications by Year in Descending Order

410 papers	5,227 citations	29 h-index	60 g-index
519 ext. papers	6,464 ext. citations	3 avg, IF	5.99 L-index

#	Paper	IF	Citations
410	Effects of Channel Length Scaling on the Signal-to-Noise Ratio in FET-Type Gas sensor with Horizontal Floating-Gate. *IEEE Electron Device Letters*, **2022**, 1-1	4.4	3
409	Impact of interlayer insulator formation methods on HfOx ferroelectricity in the metal□ferroelectric□insulator□semiconductor stack. *Applied Physics Letters*, **2022**, 120, 012901	3.4	1
408	Effects of High-Pressure Annealing on the Low-Frequency Noise Characteristics in Ferroelectric FET. *IEEE Electron Device Letters*, **2022**, 43, 13-16	4.4	9
407	Comprehensive and accurate analysis of the working principle in ferroelectric tunnel junctions using low-frequency noise spectroscopy.. *Nanoscale*, **2022**,	7.7	6
406	Variation-tolerant Capacitive Array for Binarized Neural Network. *IEEE Electron Device Letters*, **2022**, 1-1	4.4	1
405	Comprehensive TCAD-Based Validation of Interface Trap-Assisted Ferroelectric Polarization in Ferroelectric-Gate Field-Effect Transistor Memory. *IEEE Transactions on Electron Devices*, **2022**, 1-6	2.9	0
404	Optimization of channel structure and bias condition for signal-to-noise ratio improvement in Si-based FET-type gas sensor with horizontal floating-gate. *Sensors and Actuators B: Chemical*, **2022**, 357, 131398	8.5	5
403	Capacitor-Based Synaptic Devices for Hardware Spiking Neural Networks. *IEEE Electron Device Letters*, **2022**, 1-1	4.4	3
402	SiO2 Fin-Based Flash Synaptic Cells in AND Array Architecture for Binary Neural Networks. *IEEE Electron Device Letters*, **2022**, 43, 142-145	4.4	4
401	Ferroelectricity of pure HfOx in metal-ferroelectric-insulator-semiconductor stacks and its memory application. *Applied Surface Science*, **2022**, 573, 151566	6.7	5
400	On-Chip Trainable Spiking Neural Networks Using Time-To-First-Spike Encoding. *IEEE Access*, **2022**, 10, 31263-31272	3.5	
399	A Fast Weight Transfer Method for Real-Time Online Learning in RRAM-Based Neuromorphic System. *IEEE Access*, **2022**, 1-1	3.5	0
398	Novel Dual Liner Process for Side-Shielded Forksheet Device With Superior Design Margin. *IEEE Transactions on Electron Devices*, **2022**, 1-4	2.9	
397	Effects of Postdeposition Annealing Ambience on NO□Gas Sensing Performance in Si-Based FET-Type Gas Sensor. *IEEE Transactions on Electron Devices*, **2022**, 1-7	2.9	3
396	Damage-induced ferroelectricity in HfOx-based thin film. *IEEE Electron Device Letters*, **2022**, 1-1	4.4	
395	Effect of weight overlap region on neuromorphic system with memristive synaptic devices. *Chaos, Solitons and Fractals*, **2022**, 157, 111999	9.3	2
394	Investigation of Device Performance for Fin Angle Optimization in FinFET and Gate-All-Around FETs for 3 nm-Node and Beyond. *IEEE Transactions on Electron Devices*, **2022**, 69, 2088-2093	2.9	1

393	Investigation of Low-Frequency Noise Characteristics of Ferroelectric Tunnel Junction: from Conduction Mechanism and Scaling Perspectives. *IEEE Electron Device Letters*, **2022**, 1-1	4.4	4
392	Effect of Program Error in Memristive Neural Network With Weight Quantization. *IEEE Transactions on Electron Devices*, **2022**, 1-7	2.9	2
391	Analog synaptic devices applied to spiking neural networks for reinforcement learning applications. *Semiconductor Science and Technology*, **2022**, 37, 075002	1.8	
390	Highly Efficient Self-Curing Method in MOSFET Using Parasitic Bipolar Junction Transistor. *IEEE Electron Device Letters*, **2022**, 1-1	4.4	1
389	Fully integrated FET-type gas sensor with optimized signal-to-noise ratio for H2S gas detection. *Sensors and Actuators B: Chemical*, **2022**, 367, 132052	8.5	2
388	Low-Power Adaptive Integrate-and-Fire Neuron Circuit Using Positive Feedback FET Co-Integrated With CMOS. *IEEE Access*, **2021**, 1-1	3.5	0
387	Multilevel switching memristor by compliance current adjustment for off-chip training of neuromorphic system. *Chaos, Solitons and Fractals*, **2021**, 153, 111587	9.3	11
386	Ferroelectric-Metal Field-Effect Transistor with Recessed Channel for 1T-DRAM Application. *IEEE Journal of the Electron Devices Society*, **2021**, 1-1	2.3	0
385	Utilization of Unsigned Inputs for NAND Flash-Based Parallel and High-Density Synaptic Architecture in Binary Neural Networks. *IEEE Journal of the Electron Devices Society*, **2021**, 1-1	2.3	
384	Effects of Process-Induced Defects on Polarization Switching in Ferroelectric Tunneling Junction Memory. *IEEE Electron Device Letters*, **2021**, 42, 323-326	4.4	9
383	Investigation of Low-Frequency Noise Characteristics in Gated Schottky Diodes. *IEEE Electron Device Letters*, **2021**, 42, 442-445	4.4	4
382	Improvement of self-heating effect in Ge vertically stacked GAA nanowire pMOSFET by utilizing Al2O3 for high-performance logic device and electrical/thermal co-design. *Japanese Journal of Applied Physics*, **2021**, 60, SCCE04	1.4	4
381	Effect of Ag source layer thickness on the switching mechanism of TiN/Ag/SiN x /TiN conductive bridging random access memory observed at sub-□A current. *Semiconductor Science and Technology* , **2021**, 36, 055014	1.8	2
380	Synaptic Device With High Rectification Ratio Resistive Switching and Its Impact on Spiking Neural Network. *IEEE Transactions on Electron Devices*, **2021**, 68, 1610-1615	2.9	2
379	Variability of DRAM Peripheral Transistor at Liquid Nitrogen Temperature. *IEEE Transactions on Electron Devices*, **2021**, 68, 1627-1632	2.9	
378	3-bit multilevel operation with accurate programming scheme in TiO/AlOmemristor crossbar array for quantized neuromorphic system. *Nanotechnology*, **2021**, 32,	3.4	14
377	Multiplexed Silicon Nanowire Tunnel FET-Based Biosensors With Optimized Multi-Sensing Currents. *IEEE Sensors Journal*, **2021**, 21, 8839-8846	4	2
376	A Systematic Compact Model Parameter Calibration with Adaptive Pattern Search Algorithm. *Applied Sciences (Switzerland)*, **2021**, 11, 4155	2.6	1

375	Nanoscale wedge resistive-switching synaptic device and experimental verification of vector-matrix multiplication for hardware neuromorphic application. *Japanese Journal of Applied Physics*, **2021**, 60, 050905	1.4	6
374	Comparison of the characteristics of semiconductor gas sensors with different transducers fabricated on the same substrate. *Sensors and Actuators B: Chemical*, **2021**, 335, 129661	8.5	10
373	Physical Unclonable Functions Using Ferroelectric Tunnel Junctions. *IEEE Electron Device Letters*, **2021**, 42, 816-819	4.4	4
372	Optimization of post-deposition annealing temperature for improved signal-to-noise ratio in In2O3 gas sensor. *Semiconductor Science and Technology*, **2021**, 36, 075007	1.8	8
371	Impacts of Program/Erase Cycling on the Low-Frequency Noise Characteristics of Reconfigurable Gated Schottky Diodes. *IEEE Electron Device Letters*, **2021**, 42, 863-866	4.4	6
370	Novel Method Enabling Forward and Backward Propagations in NAND Flash Memory for On-Chip Learning. *IEEE Transactions on Electron Devices*, **2021**, 68, 3365-3370	2.9	1
369	Improved signal-to-noise-ratio of FET-type gas sensors using body bias control and embedded micro-heater. *Sensors and Actuators B: Chemical*, **2021**, 329, 129166	8.5	13
368	Hardware-based spiking neural network architecture using simplified backpropagation algorithm and homeostasis functionality. *Neurocomputing*, **2021**, 428, 153-165	5.4	2
367	Low-power and reliable gas sensing system based on recurrent neural networks. *Sensors and Actuators B: Chemical*, **2021**, 340, 129258	8.5	7
366	Improvement in Self-Heating Characteristic by Incorporating Hetero-Gate-Dielectric in Gate-All-Around MOSFETs. *IEEE Journal of the Electron Devices Society*, **2021**, 9, 36-41	2.3	9
365	Effect of charge storage engineering on the NO gas sensing properties of a WO FET-type gas sensor with a horizontal floating-gate. *Nanoscale*, **2021**, 13, 9009-9017	7.7	8
364	Integrate-and-Fire Neuron Circuit With Synaptic Off-Current Blocking Operation. *IEEE Access*, **2021**, 9, 127841-127851	3.5	
363	Double-Gated Ferroelectric-Gate Field-Effect-Transistor for Processing in Memory. *IEEE Electron Device Letters*, **2021**, 1-1	4.4	0
362	Improved rectification characteristics by engineering energy barrier height in TiOx-based RRAM. *Microelectronic Engineering*, **2021**, 237, 111498	2.5	0
361	Selected Bit-Line Current PUF: Implementation of Hardware Security Primitive Based on a Memristor Crossbar Array. *IEEE Access*, **2021**, 9, 120901-120910	3.5	0
360	Hardware-Based Spiking Neural Network Using a TFT-Type AND Flash Memory Array Architecture Based on Direct Feedback Alignment. *IEEE Access*, **2021**, 9, 73121-73132	3.5	4
359	Spiking Neural Networks With Time-to-First-Spike Coding Using TFT-Type Synaptic Device Model. *IEEE Access*, **2021**, 9, 78098-78107	3.5	2
358	Suppression of Statistical Variability in Stacked Nanosheet Using Floating Fin Structure. *IEEE Electron Device Letters*, **2021**, 1-1	4.4	

357	Effect of Random Dopant Fluctuation on Data Retention Time Distribution in DRAM. *IEEE Transactions on Electron Devices*, **2021**, 1-6	2.9	0
356	Trap-Induced Data-Retention-Time Degradation of DRAM and Improvement Using Dual Work-Function Metal Gate. *IEEE Electron Device Letters*, **2021**, 42, 38-41	4.4	3
355	Quantized Weight Transfer Method Using Spike-Timing-Dependent Plasticity for Hardware Spiking Neural Network. *Applied Sciences (Switzerland)*, **2021**, 11, 2059	2.6	1
354	Low-Latency Spiking Neural Networks Using Pre-Charged Membrane Potential and Delayed Evaluation. *Frontiers in Neuroscience*, **2021**, 15, 629000	5.1	0
353	On-chip trainable hardware-based deep Q-networks approximating a backpropagation algorithm. *Neural Computing and Applications*, **2021**, 33, 9391-9402	4.8	1
352	Response Comparison of Resistor- and Si FET-Type Gas Sensors on the Same Substrate. *IEEE Transactions on Electron Devices*, **2021**, 68, 3552-3557	2.9	0
351	Direct Gradient Calculation: Simple and Variation-Tolerant On-Chip Training Method for Neural Networks. *Advanced Intelligent Systems*, **2021**, 3, 2100064	6	0
350	Effect of Lateral Charge Diffusion on Retention Characteristics of 3D NAND Flash Cells. *IEEE Electron Device Letters*, **2021**, 42, 1148-1151	4.4	0
349	3-D AND-Type Flash Memory Architecture With High-□Gate Dielectric for High-Density Synaptic Devices. *IEEE Transactions on Electron Devices*, **2021**, 68, 3801-3806	2.9	3
348	Hardware-Based Spiking Neural Networks Using Capacitor-Less Positive Feedback Neuron Devices. *IEEE Transactions on Electron Devices*, **2021**, 68, 4766-4772	2.9	
347	A novel physical unclonable function (PUF) using 16□16 pure-HfOferroelectric tunnel junction array for security applications. *Nanotechnology*, **2021**, 32,	3.4	2
346	Gate-First Negative Capacitance Field-Effect Transistor With Self-Aligned Nickel-Silicide Source and Drain. *IEEE Transactions on Electron Devices*, **2021**, 68, 4754-4757	2.9	0
345	A More Hardware-Oriented Spiking Neural Network Based on Leading Memory Technology and Its Application With Reinforcement Learning. *IEEE Transactions on Electron Devices*, **2021**, 68, 4411-4417	2.9	3
344	Interlayer engineering for enhanced ferroelectric tunnel junction operations in HfO-based metal-ferroelectric-insulator-semiconductor stack. *Nanotechnology*, **2021**, 32,	3.4	4
343	Efficient fusion of spiking neural networks and FET-type gas sensors for a fast and reliable artificial olfactory system. *Sensors and Actuators B: Chemical*, **2021**, 345, 130419	8.5	4
342	On-chip adaptive matching learning with charge-trap synapse device and ReLU activation circuit. *Solid-State Electronics*, **2021**, 186, 108177	1.7	0
341	Vertically-Stacked Si0.2Ge0.8 Nanosheet Tunnel FET With 70 mV/Dec Average Subthreshold Swing. *IEEE Electron Device Letters*, **2021**, 1-1	4.4	2
340	Improvement of Resistive Switching Characteristics of Titanium Oxide Based Nanowedge RRAM Through Nickel Silicidation. *IEEE Transactions on Electron Devices*, **2021**, 68, 438-442	2.9	1

339	Core-Shell Dual-Gate Nanowire Memory as a Synaptic Device for Neuromorphic Application. *IEEE Journal of the Electron Devices Society*, **2021**, 1-1	2.3	1
338	Fabrication and Characterization of TiOx Memristor for Synaptic Device Application. *IEEE Nanotechnology Magazine*, **2020**, 19, 475-480	2.6	7
337	Memristive and Synaptic Characteristics of Nitride-Based Heterostructures on Si Substrate. *Nanomaterials*, **2020**, 10,	5.4	11
336	Ferroelectric-Gate Field-Effect Transistor Memory With Recessed Channel. *IEEE Electron Device Letters*, **2020**, 41, 1201-1204	4.4	13
335	Analysis on Reverse Drain-Induced Barrier Lowering and Negative Differential Resistance of Ferroelectric-Gate Field-Effect Transistor Memory. *IEEE Electron Device Letters*, **2020**, 41, 1197-1200	4.4	6
334	Investigation of the Thermal Recovery From Reset Breakdown of a SiNx-Based RRAM. *IEEE Transactions on Electron Devices*, **2020**, 67, 1600-1605	2.9	6
333	Investigation of Sidewall High-k Interfacial Layer Effect in Gate-All-Around Structure. *IEEE Transactions on Electron Devices*, **2020**, 67, 1859-1863	2.9	7
332	Effect of Word-Line Bias on Linearity of Multi-Level Conductance Steps for Multi-Layer Neural Networks Based on NAND Flash Cells. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 4138-4142	1.3	2
331	Synaptic Characteristics of Amorphous Boron Nitride-Based Memristors on a Highly Doped Silicon Substrate for Neuromorphic Engineering. *ACS Applied Materials & Interfaces*, **2020**, 12, 33908-33916	9.5	24
330	Filamentary and interface switching of CMOS-compatible Ta2O5 memristor for non-volatile memory and synaptic devices. *Applied Surface Science*, **2020**, 529, 147167	6.7	20
329	Vertical Inner Gate Transistors for 4F2 DRAM Cell. *IEEE Transactions on Electron Devices*, **2020**, 67, 944-948	2.9	3
328	Negative Capacitance Effect on MOS Structure: Influence of Electric Field Variation. *IEEE Nanotechnology Magazine*, **2020**, 19, 168-171	2.6	6
327	Impact of the Sub-Resting Membrane Potential on Accurate Inference in Spiking Neural Networks. *Scientific Reports*, **2020**, 10, 3515	4.9	6
326	Extension of the DG Model to the Second-Order Quantum Correction for Analysis of the Single-Charge Effect in Sub-10-nm MOS Devices. *IEEE Journal of the Electron Devices Society*, **2020**, 1-1	2.3	3
325	HfO x -based nano-wedge structured resistive switching memory device operating at sub-A current for neuromorphic computing application. *Semiconductor Science and Technology*, **2020**, 35, 055002	1.8	2
324	Design and Optimization of Triple-k Spacer Structure in Two-Stack Nanosheet FET From OFF-State Leakage Perspective. *IEEE Transactions on Electron Devices*, **2020**, 67, 1317-1322	2.9	9
323	Analog Complementary Metal-Oxide-Semiconductor Integrate-and-Fire Neuron Circuit for Overflow Retaining in Hardware Spiking Neural Networks. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 3117-3122	1.3	5
322	A Simulation Study on Reducing the Grain Boundary Position Dependency in Tunneling Thin-Film Transistors Using a Wide Tunneling Area. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 6627-6631	1.3	

321	Insertion of Ag Layer in TiN/SiNx/TiN RRAM and Its Effect on Filament Formation Modeled by Monte Carlo Simulation. *IEEE Access*, **2020**, 8, 228720-228730	3.5	3
320	Investigation of Electrical Characteristic Behavior Induced by Channel-Release Process in Stacked Nanosheet Gate-All-Around MOSFETs. *IEEE Transactions on Electron Devices*, **2020**, 67, 2648-2652	2.9	15
319	Electrical and Thermal Performances of Omega-Shaped-Gate Nanowire Field Effect Transistors for Low Power Operation. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 4092-4096	1.3	8
318	Implementation of Synaptic Device Using Various High- Gate Dielectric Stacks. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 4292-4297	1.3	3
317	I-Shaped SiGe Fin Tunnel Field-Effect Transistor with High / Ratio. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 4298-4302	1.3	
316	Suppression of reverse drain induced barrier lowering in negative capacitance FDSOI field effect transistor using oxide charge trapping layer. *Semiconductor Science and Technology*, **2020**, 35, 125003	1.8	3
315	A Novel Vector-matrix Multiplication (VMM) Architecture based on NAND Memory Array. *Journal of Semiconductor Technology and Science*, **2020**, 20, 242-248	1.5	7
314	Detection of Thermal Transport on Chip Using Gate-Induced Drain Leakage Current. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 4980-4984	1.3	
313	Efficient precise weight tuning protocol considering variation of the synaptic devices and target accuracy. *Neurocomputing*, **2020**, 378, 189-196	5.4	6
312	Simulation of the effect of parasitic channel height on characteristics of stacked gate-all-around nanosheet FET. *Solid-State Electronics*, **2020**, 164, 107686	1.7	12
311	Field Effect Transistor-Type Devices Using High-□Gate Insulator Stacks for Neuromorphic Applications. *ACS Applied Electronic Materials*, **2020**, 2, 323-328	4	4
310	Surface Ge-rich p-type SiGe channel tunnel field-effect transistor fabricated by local condensation technique. *Solid-State Electronics*, **2020**, 164, 107701	1.7	11
309	Solving Overlapping Pattern Issues in On-Chip Learning of Bio-Inspired Neuromorphic System with Synaptic Transistors. *Electronics (Switzerland)*, **2020**, 9, 13	2.6	3
308	3D Integrable W/SiN/n-Si/p-Si 1D1R Unipolar Resistive Random Access Memory Synapse for Suppressing Reverse Leakage in Spiking Neural Network. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 4735-4739	1.3	4
307	Pruning for Hardware-Based Deep Spiking Neural Networks Using Gated Schottky Diode as Synaptic Devices. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 6603-6608	1.3	1
306	More physical understanding of current characteristics of tunneling field-effect transistor leveraged by gate positions and properties through dual-gate and gate-all-around structuring. *Applied Physics A: Materials Science and Processing*, **2020**, 126, 1	2.6	
305	Reset-voltage-dependent precise tuning operation of TiOx/Al2O3 memristive crossbar array. *Applied Physics Letters*, **2020**, 117, 152103	3.4	24
304	Zinc Tin Oxide Synaptic Device for Neuromorphic Engineering. *IEEE Access*, **2020**, 8, 130678-130686	3.5	17

303	Analysis of a Schottky Barrier MOSFET for Synaptic Device Using Hot Carrier Injection. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 6592-6595	1.3	
302	On-Chip Training Spiking Neural Networks Using Approximated Backpropagation With Analog Synaptic Devices. *Frontiers in Neuroscience*, **2020**, 14, 423	5.1	20
301	Current suppressed self-compliance characteristics of oxygen rich TiOy inserted Al2O3/TiOx based RRAM. *Applied Physics Letters*, **2020**, 117, 202106	3.4	16
300	Realization of Biomimetic Synaptic Functions in a One-Cell Organic Resistive Switching Device Using the Diffusive Parameter of Conductive Filaments. *ACS Applied Materials & Interfaces*, **2020**, 12, 51719-51728	9.5	8
299	A Quantum-Well Charge-Trap Synaptic Transistor With Highly Linear Weight Tunability. *IEEE Journal of the Electron Devices Society*, **2020**, 8, 834-840	2.3	3
298	Vertically Stacked Gate-All-Around Structured Tunneling-Based Ternary-CMOS. *IEEE Transactions on Electron Devices*, **2020**, 67, 3889-3893	2.9	5
297	Investigation on Tunneling-based Ternary CMOS with Ferroelectric-Gate Field Effect Transistor Using TCAD Simulation. *Applied Sciences (Switzerland)*, **2020**, 10, 4977	2.6	2
296	Multilevel Switching Characteristics of Si3N4-Based Nano-Wedge Resistive Switching Memory and Array Simulation for In-Memory Computing Application. *Electronics (Switzerland)*, **2020**, 9, 1228	2.6	4
295	. *IEEE Transactions on Electron Devices*, **2020**, 67, 4541-4544	2.9	4
294	AND Flash Array Based on Charge Trap Flash for Implementation of Convolutional Neural Networks. *IEEE Electron Device Letters*, **2020**, 41, 1653-1656	4.4	18
293	3D AND-Type Stacked Array for Neuromorphic Systems. *Micromachines*, **2020**, 11,	3.3	2
292	Proposition of deposition and bias conditions for optimal signal-to-noise-ratio in resistor- and FET-type gas sensors. *Nanoscale*, **2020**, 12, 19768-19775	7.7	19
291	Sensitivity Analysis Based on Neural Network for Optimizing Device Characteristics. *IEEE Electron Device Letters*, **2020**, 41, 1548-1551	4.4	6
290	. *IEEE Access*, **2020**, 8, 202639-202647	3.5	6
289	Double-Gated Asymmetric Floating-Gate-Based Synaptic Device for Effective Performance Enhancement Through Online Learning. *IEEE Access*, **2020**, 8, 217735-217743	3.5	
288	Input-modulating adaptive neuron circuit employing asymmetric floating-gate MOSFET with two independent control gates. *Solid-State Electronics*, **2020**, 163, 107667	1.7	5
287	Low frequency noise characteristics of resistor- and Si MOSFET-type gas sensors fabricated on the same Si wafer with In2O3 sensing layer. *Sensors and Actuators B: Chemical*, **2020**, 318, 128087	8.5	25
286	Tunneling oxide engineering for improving retention in nonvolatile charge-trapping memory with TaN/Al2O3/HfO2/SiO2/Al2O3/SiO2/Si structure. *Japanese Journal of Applied Physics*, **2020**, 59, 061006	1.4	5

285	A Spiking Neural Network with a Global Self-Controller for Unsupervised Learning Based on Spike-Timing-Dependent Plasticity Using Flash Memory Synaptic Devices **2019**,		5
284	Operation Scheme of Multi-Layer Neural Networks Using NAND Flash Memory as High-Density Synaptic Devices. *IEEE Journal of the Electron Devices Society*, **2019**, 7, 1085-1093	2.3	16
283	Characterization of a Capacitorless DRAM Cell for Cryogenic Memory Applications. *IEEE Electron Device Letters*, **2019**, 40, 1614-1617	4.4	5
282	Oxide Thin Film Transistor With a Novel Gate Insulator Stack to Suppress Photo-Excited Charge Injection. *IEEE Nanotechnology Magazine*, **2019**, 18, 491-493	2.6	2
281	Partial Isolation Type Saddle-FinFET(Pi-FinFET) for Sub-30 nm DRAM Cell Transistors. *Electronics (Switzerland)*, **2019**, 8, 8	2.6	5
280	Si-Based FET-Type Synaptic Device With Short-Term and Long-Term Plasticity Using High- $kappa$ Gate-Stack. *IEEE Transactions on Electron Devices*, **2019**, 66, 917-923	2.9	9
279	Demonstration of Fin-Tunnel Field-Effect Transistor with Elevated Drain. *Micromachines*, **2019**, 10,	3.3	9
278	Resistive random-access memory with an a-Si/SiNx double-layer. *Solid-State Electronics*, **2019**, 158, 64-69	1.7	2
277	Analysis of Hot Carrier Injection According to Gate Length. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6746-6749	1.3	1
276	SiO2 layer effect on atomic layer deposition Al2O3-based resistive switching memory. *Applied Physics Letters*, **2019**, 114, 182102	3.4	11
275	Highly Reliable Inference System of Neural Networks Using Gated Schottky Diodes. *IEEE Journal of the Electron Devices Society*, **2019**, 7, 522-528	2.3	9
274	Effect of Nitrogen Content in Tunneling Dielectric on Cell Properties of 3-D NAND Flash Cells. *IEEE Electron Device Letters*, **2019**, 40, 702-705	4.4	5
273	Nonvolatile Memory (NVM) Operation of Tunnel Field-Effect Transistor (TFET) Using Ferroelectric HfO□ Sidewall. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6061-6065	1.3	
272	Simulation Program with Integrated Circuit Emphasis Compact Modeling of a Dual-Gate Positive-Feedback Field-Effect Transistor for Circuit Simulations. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6417-6421	1.3	0
271	Analysis of Minority Carrier Lifetime Dependence on Dual Gate Feedback Field Effect Transistor. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6767-6770	1.3	1
270	Partial Contact Etching and Gate Lowering on Tunneling Field Effect Transistor for Performance and Power Enhancement. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6808-6811	1.3	
269	Near-Linear Potentiation Mechanism of Gated Schottky Diode as a Synaptic Device. *IEEE Journal of the Electron Devices Society*, **2019**, 7, 335-343	2.3	4
268	Synaptic device using a floating fin-body MOSFET with memory functionality for neural network. *Solid-State Electronics*, **2019**, 156, 23-27	1.7	3

267	A Band-Engineered One-Transistor DRAM With Improved Data Retention and Power Efficiency. *IEEE Electron Device Letters*, **2019**, 40, 562-565	4.4	11
266	Double-Gate TFET With Vertical Channel Sandwiched by Lightly Doped Si. *IEEE Transactions on Electron Devices*, **2019**, 66, 1656-1661	2.9	40
265	Adaptive learning rule for hardware-based deep neural networks using electronic synapse devices. *Neural Computing and Applications*, **2019**, 31, 8101-8116	4.8	29
264	Reversible nonvolatile and threshold switching characteristics in Cu/high-k/Si devices. *IEICE Electronics Express*, **2019**, 16, 20190404-20190404	0.5	1
263	Analysis on New Read Disturbance Induced by Hot Carrier Injections in 3-D Channel-Stacked NAND Flash Memory. *IEEE Transactions on Electron Devices*, **2019**, 66, 3326-3330	2.9	3
262	Implementation of Boolean Logic Functions in Charge Trap Flash for In-Memory Computing. *IEEE Electron Device Letters*, **2019**, 40, 1358-1361	4.4	10
261	Polysilicon-Based Synaptic Transistor and Array Structure for Short/Long-Term Memory. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6066-6069	1.3	1
260	A new device characteristic model generation by machine learning **2019**,		2
259	Tunnel Field Effect Transistor with Ferroelectric Gate Insulator. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6095-6098	1.3	2
258	Grayscale Image Recognition Using Spike-Rate-Based Online Learning and Threshold Adjustment of Neurons in a Thin-Film Transistor-Type NOR Flash Memory Array. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6055-6060	1.3	2
257	Transient Analysis of Tunnel Field-Effect Transistor with Raised Drain. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6212-6216	1.3	1
256	Unsupervised Online Learning With Multiple Postsynaptic Neurons Based on Spike-Timing-Dependent Plasticity Using a Thin-Film Transistor-Type NOR Flash Memory Array. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6050-6054	1.3	7
255	An Online Learning Method Using Spike-Timing Dependent Plasticity for Neuromorphic Systems. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6776-6780	1.3	1
254	Overflow Handling Integrate-and-Fire Silicon-on-Insulator Neuron Circuit Incorporating a Schmitt Trigger Implemented by Back-Gate Effect. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6183-6186	1.3	7
253	A systematic model parameter extraction using differential evolution searching **2019**,		2
252	A Low-Energy High-Density Capacitor-Less I&F Neuron Circuit Using Feedback FET Co-Integrated With CMOS. *IEEE Journal of the Electron Devices Society*, **2019**, 1-1	2.3	7
251	Reconfigurable Field-Effect Transistor as a Synaptic Device for XNOR Binary Neural Network. *IEEE Electron Device Letters*, **2019**, 40, 624-627	4.4	13
250	High-Density and Highly-Reliable Binary Neural Networks Using NAND Flash Memory Cells as Synaptic Devices **2019**,		20

249	Investigation on Ambipolar Current Suppression Using a Stacked Gate in an L-shaped Tunnel Field-Effect Transistor. *Micromachines*, **2019**, 10,	3.3	3
248	Ni/GeOx/p+ Si resistive-switching random-access memory with full Si processing compatibility and its characterization and modeling. *Vacuum*, **2019**, 161, 63-70	3.7	3
247	Design and Characterization of Semi-Floating-Gate Synaptic Transistor. *Micromachines*, **2019**, 10,	3.3	8
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