Byung-Gook Park

List of Publications by Citations

410 papers	5,227 citations	29 h-index	60 g-index
519 ext. papers	6,464 ext. citations	3 avg, IF	5.99 L-index

#	Paper	IF	Citations
410	Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec. *IEEE Electron Device Letters*, **2007**, 28, 743-745	4.4	1160
409	Demonstration of L-Shaped Tunnel Field-Effect Transistors. *IEEE Transactions on Electron Devices*, **2016**, 63, 1774-1778	2.9	161
408	A three-dimensional simulation of quantum transport in silicon nanowire transistor in the presence of electron-phonon interactions. *Journal of Applied Physics*, **2006**, 99, 123719	2.5	153
407	Analog Synaptic Behavior of a Silicon Nitride Memristor. *ACS Applied Materials & Interfaces*, **2017**, 9, 40420-40427	9.5	137
406	A new charge pump without degradation in threshold voltage due to body effect [memory applications]. *IEEE Journal of Solid-State Circuits*, **2000**, 35, 1227-1230	5.5	118
405	Hysteresis mechanism and reduction method in the bottom-contact pentacene thin-film transistors with cross-linked poly(vinyl alcohol) gate insulator. *Applied Physics Letters*, **2006**, 88, 252102	3.4	76
404	Resistive switching characteristics of Si3N4-based resistive-switching random-access memory cell with tunnel barrier for high density integration and low-power applications. *Applied Physics Letters*, **2015**, 106, 212106	3.4	69
403	Design optimization of gate-all-around (GAA) MOSFETs. *IEEE Nanotechnology Magazine*, **2006**, 5, 186-191	2.6	68
402	Neuronal dynamics in HfO/AlO-based homeothermic synaptic memristors with low-power and homogeneous resistive switching. *Nanoscale*, **2018**, 11, 237-245	7.7	63
401	Nonlinear and multilevel resistive switching memory in Ni/Si3N4/Al2O3/TiN structures. *Applied Physics Letters*, **2016**, 108, 212103	3.4	58
400	Scaling Effect on Silicon Nitride Memristor with Highly Doped Si Substrate. *Small*, **2018**, 14, e1704062	11	55
399	Hysteresis mechanism in pentacene thin-film transistors with poly(4-vinyl phenol) gate insulator. *Applied Physics Letters*, **2006**, 89, 262120	3.4	54
398	Silicon-Based Floating-Body Synaptic Transistor With Frequency-Dependent Short- and Long-Term Memories. *IEEE Electron Device Letters*, **2016**, 37, 249-252	4.4	52
397	Silicon synaptic transistor for hardware-based spiking neural network and neuromorphic system. *Nanotechnology*, **2017**, 28, 405202	3.4	52
396	100-nm n-/p-channel I-MOS using a novel self-aligned structure. *IEEE Electron Device Letters*, **2005**, 26, 261-263	4.4	51
395	. *IEEE Transactions on Electron Devices*, **2012**, 59, 35-45	2.9	50
394	Accurate analysis of conduction and resistive-switching mechanisms in double-layered resistive-switching memory devices. *Applied Physics Letters*, **2012**, 101, 103506	3.4	50

393	Charge decay characteristics of silicon-oxide-nitride-oxide-silicon structure at elevated temperatures and extraction of the nitride trap density distribution. *Applied Physics Letters*, **2004**, 85, 660-662	3.4	48
392	Understanding rectifying and nonlinear bipolar resistive switching characteristics in Ni/SiNx/p-Si memory devices. *RSC Advances*, **2017**, 7, 17882-17888	3.7	43
391	Spiking Neural Network Using Synaptic Transistors and Neuron Circuits for Pattern Recognition With Noisy Images. *IEEE Electron Device Letters*, **2018**, 39, 630-633	4.4	42
390	Double-Gate TFET With Vertical Channel Sandwiched by Lightly Doped Si. *IEEE Transactions on Electron Devices*, **2019**, 66, 1656-1661	2.9	40
389	Comprehensive analysis of retention characteristics in 3-D NAND flash memory cells with tube-type poly-Si channel structure **2015**,		40
388	High-Density and Near-Linear Synaptic Device Based on a Reconfigurable Gated Schottky Diode. *IEEE Electron Device Letters*, **2017**, 38, 1153-1156	4.4	38
387	. *IEEE Transactions on Electron Devices*, **2011**, 58, 1127-1133	2.9	34
386	A New Capacitorless 1T DRAM Cell: Surrounding Gate MOSFET With Vertical Channel (SGVC Cell). *IEEE Nanotechnology Magazine*, **2007**, 6, 352-357	2.6	31
385	Low hysteresis pentacene thin-film transistors using SiO2/cross-linked poly(vinyl alcohol) gate dielectric. *Applied Physics Letters*, **2006**, 89, 263507	3.4	31
384	Silicon single-electron transistors with sidewall depletion gates and their application to dynamic single-electron transistor logic. *IEEE Transactions on Electron Devices*, **2002**, 49, 627-635	2.9	31
383	Fully Si compatible SiN resistive switching memory with large self-rectification ratio. *AIP Advances*, **2016**, 6, 015021	1.5	31
382	Silicon-compatible compound semiconductor tunneling field-effect transistor for high performance and low standby power operation. *Applied Physics Letters*, **2011**, 99, 243505	3.4	30
381	Adaptive learning rule for hardware-based deep neural networks using electronic synapse devices. *Neural Computing and Applications*, **2019**, 31, 8101-8116	4.8	29
380	Threshold Voltage Fluctuation by Random Telegraph Noise in Floating Gate nand Flash Memory String. *IEEE Transactions on Electron Devices*, **2011**, 58, 67-73	2.9	29
379	Compact Design of Low Power Standard Ternary Inverter Based on OFF-State Current Mechanism Using Nano-CMOS Technology. *IEEE Transactions on Electron Devices*, **2015**, 62, 2396-2403	2.9	28
378	3-D Floating-Gate Synapse Array With Spike-Time-Dependent Plasticity. *IEEE Transactions on Electron Devices*, **2018**, 65, 101-107	2.9	28
377	Fabrication and program/erase characteristics of 30-nm SONOS nonvolatile memory devices. *IEEE Nanotechnology Magazine*, **2003**, 2, 258-264	2.6	28
376	A Simple Figure of Merit of RF MOSFET for Low-Noise Amplifier Design. *IEEE Electron Device Letters* , **2008**, 29, 1380-1382	4.4	27

375	Gradual bipolar resistive switching in Ni/Si3N4/n+-Si resistive-switching memory device for high-density integration and low-power applications. *Solid-State Electronics*, **2015**, 114, 94-97	1.7	26
374	Improved resistive switching characteristics in Ni/SiNx/p++-Si devices by tuning x. *Applied Physics Letters*, **2017**, 111, 033509	3.4	26
373	Ultralow power switching in a silicon-rich SiN/SiN double-layer resistive memory device. *Physical Chemistry Chemical Physics*, **2017**, 19, 18988-18995	3.6	25
372	Three-Dimensional NAND Flash Memory Based on Single-Crystalline Channel Stacked Array. *IEEE Electron Device Letters*, **2013**, 34, 990-992	4.4	25
371	Low frequency noise characteristics of resistor- and Si MOSFET-type gas sensors fabricated on the same Si wafer with In2O3 sensing layer. *Sensors and Actuators B: Chemical*, **2020**, 318, 128087	8.5	25
370	Synaptic Characteristics of Amorphous Boron Nitride-Based Memristors on a Highly Doped Silicon Substrate for Neuromorphic Engineering. *ACS Applied Materials & Interfaces*, **2020**, 12, 33908-33916	9.5	24
369	System-Level Simulation of Hardware Spiking Neural Network Based on Synaptic Transistors and I&F Neuron Circuits. *IEEE Electron Device Letters*, **2018**, 39, 1441-1444	4.4	24
368	Modeling and Parameter Extraction for the Series Resistance in Thin-Film Transistors. *IEEE Transactions on Electron Devices*, **2009**, 56, 431-440	2.9	24
367	Enhancement of Memory Performance Using Doubly Stacked Si-Nanocrystal Floating Gates Prepared by Ion Beam Sputtering in UHV. *IEEE Transactions on Electron Devices*, **2007**, 54, 359-362	2.9	24
366	A practical SPICE model based on the physics and characteristics of realistic single-electron transistors. *IEEE Nanotechnology Magazine*, **2002**, 1, 226-232	2.6	24
365	A New Programming Method to Alleviate the Program Speed Variation in Three-Dimensional Stacked Array NAND Flash Memory. *Journal of Semiconductor Technology and Science*, **2014**, 14, 566-571	1.5	24
364	Reset-voltage-dependent precise tuning operation of TiOx/Al2O3 memristive crossbar array. *Applied Physics Letters*, **2020**, 117, 152103	3.4	24
363	Nano-cone resistive memory for ultralow power operation. *Nanotechnology*, **2017**, 28, 125207	3.4	23
362	A study on the carrier injection mechanism of the bottom-contact pentacene thin film transistor. *Applied Physics Letters*, **2010**, 96, 103305	3.4	23
361	Admittance Measurements on OFET Channel and Its Modeling With R₿C$ Network. *IEEE Electron Device Letters*, **2007**, 28, 204-206	4.4	23
360	3-D Stacked Synapse Array Based on Charge-Trap Flash Memory for Implementation of Deep Neural Networks. *IEEE Transactions on Electron Devices*, **2019**, 66, 420-427	2.9	22
359	Implementation of Short-Term Plasticity and Long-Term Potentiation in a Synapse Using Si-Based Type of Charge-Trap Memory. *IEEE Transactions on Electron Devices*, **2015**, 62, 569-573	2.9	21
358	Complementary Silicon Nanowire Hydrogen Ion Sensor With High Sensitivity and Voltage Output. *IEEE Electron Device Letters*, **2012**, 33, 1768-1770	4.4	21

357	Single-Crystalline Si STacked ARray (STAR) NAND Flash Memory. *IEEE Transactions on Electron Devices*, **2011**, 58, 1006-1014	2.9	21
356	Effects of Localized Body Doping on Switching Characteristics of Tunnel FET Inverters With Vertical Structures. *IEEE Transactions on Electron Devices*, **2017**, 64, 1799-1805	2.9	20
355	Compact Neuromorphic System With Four-Terminal Si-Based Synaptic Devices for Spiking Neural Networks. *IEEE Transactions on Electron Devices*, **2017**, 64, 2438-2444	2.9	20
354	Filamentary and interface switching of CMOS-compatible Ta2O5 memristor for non-volatile memory and synaptic devices. *Applied Surface Science*, **2020**, 529, 147167	6.7	20
353	70-nm impact-ionization metal-oxide-semiconductor (I-MOS) devices integrated with tunneling field-effect transistors (TFETs)		20
352	On-Chip Training Spiking Neural Networks Using Approximated Backpropagation With Analog Synaptic Devices. *Frontiers in Neuroscience*, **2020**, 14, 423	5.1	20
351	High-Density and Highly-Reliable Binary Neural Networks Using NAND Flash Memory Cells as Synaptic Devices **2019**,		20
350	Integrate-and-fire neuron circuit using positive feedback field effect transistor for low power operation. *Journal of Applied Physics*, **2018**, 124, 152107	2.5	20
349	The Compact Modeling of Channel Potential in Sub-30-nm NAND Flash Cell String. *IEEE Electron Device Letters*, **2012**, 33, 321-323	4.4	19
348	An Accurate Compact Model Considering Direct-Channel Interference of Adjacent Cells in Sub-30-nm nand Flash Technologies. *IEEE Electron Device Letters*, **2012**, 33, 1114-1116	4.4	19
347	Proposition of deposition and bias conditions for optimal signal-to-noise-ratio in resistor- and FET-type gas sensors. *Nanoscale*, **2020**, 12, 19768-19775	7.7	19
346	Effects of conducting defects on resistive switching characteristics of SiNx-based resistive random-access memory with MIS structure. *Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics*, **2015**, 33, 062201	1.3	18
345	Self-gating effects in carbon nanotube network based liquid gate field effect transistors. *Applied Physics Letters*, **2008**, 93, 243115	3.4	18
344	Electrical characteristics of FinFET with vertically nonuniform source/drain doping profile. *IEEE Nanotechnology Magazine*, **2002**, 1, 233-237	2.6	18
343	AND Flash Array Based on Charge Trap Flash for Implementation of Convolutional Neural Networks. *IEEE Electron Device Letters*, **2020**, 41, 1653-1656	4.4	18
342	Adaptive Weight Quantization Method for Nonlinear Synaptic Devices. *IEEE Transactions on Electron Devices*, **2019**, 66, 395-401	2.9	18
341	A Proposal on an Optimized Device Structure With Experimental Studies on Recent Devices for the DRAM Cell Transistor. *IEEE Transactions on Electron Devices*, **2007**, 54, 3325-3335	2.9	17
340	Zinc Tin Oxide Synaptic Device for Neuromorphic Engineering. *IEEE Access*, **2020**, 8, 130678-130686	3.5	17

339	Operation Scheme of Multi-Layer Neural Networks Using NAND Flash Memory as High-Density Synaptic Devices. *IEEE Journal of the Electron Devices Society*, **2019**, 7, 1085-1093	2.3	16
338	Vertical type double gate tunnelling FETs with thin tunnel barrier. *Electronics Letters*, **2015**, 51, 718-720	1.1	16
337	Current suppressed self-compliance characteristics of oxygen rich TiOy inserted Al2O3/TiOx based RRAM. *Applied Physics Letters*, **2020**, 117, 202106	3.4	16
336	Uniformity Improvement of SiNx-Based Resistive Switching Memory by Suppressed Internal Overshoot Current. *IEEE Nanotechnology Magazine*, **2018**, 17, 824-828	2.6	15
335	Twin SONOS memory with 30-nm storage nodes under a merged gate fabricated with inverted sidewall and damascene process. *IEEE Electron Device Letters*, **2004**, 25, 317-319	4.4	15
334	Investigation of Electrical Characteristic Behavior Induced by Channel-Release Process in Stacked Nanosheet Gate-All-Around MOSFETs. *IEEE Transactions on Electron Devices*, **2020**, 67, 2648-2652	2.9	15
333	Investigation on the characteristics of stress-induced hump in amorphous oxide thin film transistors. *Applied Physics Letters*, **2011**, 99, 043502	3.4	14
332	Threshold-Voltage Modeling of Body-Tied FinFETs (Bulk FinFETs). *IEEE Transactions on Electron Devices*, **2007**, 54, 537-545	2.9	14
331	The effects of deuterium annealing on the reduction of dark currents in the CMOS APS. *IEEE Transactions on Electron Devices*, **2004**, 51, 1346-1349	2.9	14
330	Ultrathin gate oxide grown on nitrogen-implanted silicon for deep submicron CMOS transistors. *IEEE Transactions on Electron Devices*, **2001**, 48, 2310-2316	2.9	14
329	3-bit multilevel operation with accurate programming scheme in TiO/AlOmemristor crossbar array for quantized neuromorphic system. *Nanotechnology*, **2021**, 32,	3.4	14
328	Ferroelectric-Gate Field-Effect Transistor Memory With Recessed Channel. *IEEE Electron Device Letters*, **2020**, 41, 1201-1204	4.4	13
327	Suppression of Read Disturb Fail Caused by Boosting Hot Carrier Injection Effect for 3-D Stack NAND Flash Memories. *IEEE Electron Device Letters*, **2014**, 35, 42-44	4.4	13
326	SiNW-CMOS Hybrid Common-Source Amplifier as a Voltage-Readout Hydrogen Ion Sensor. *IEEE Electron Device Letters*, **2013**, 34, 135-137	4.4	13
325	Independent Double-Gate Fin SONOS Flash Memory Fabricated With Sidewall Spacer Patterning. *IEEE Transactions on Electron Devices*, **2009**, 56, 1721-1728	2.9	13
324	Investigation of Gate Etch Damage at Metal/High-k Gate Dielectric Stack Through Random Telegraph Noise in Gate Edge Direct Tunneling Current. *IEEE Electron Device Letters*, **2011**, 32, 569-571	4.4	13
323	SET/CMOS hybrid process and multiband filtering circuits. *IEEE Transactions on Electron Devices*, **2005**, 52, 1845-1850	2.9	13
322	Reconfigurable Field-Effect Transistor as a Synaptic Device for XNOR Binary Neural Network. *IEEE Electron Device Letters*, **2019**, 40, 624-627	4.4	13

321	Improved signal-to-noise-ratio of FET-type gas sensors using body bias control and embedded micro-heater. *Sensors and Actuators B: Chemical*, **2021**, 329, 129166	8.5	13
320	Power- and Low-Resistance-State-Dependent, Bipolar Reset-Switching Transitions in SiN-Based Resistive Random-Access Memory. *Nanoscale Research Letters*, **2016**, 11, 360	5	12
319	Self-Compliant Bipolar Resistive Switching in SiN-Based Resistive Switching Memory. *Materials*, **2017**, 10,	3.5	12
318	Effect of traps on transient bit-line current behavior in word-line stacked nand flash memory with poly-Si body **2014**,		12
317	Design and Fabrication of Asymmetric MOSFETs Using a Novel Self-Aligned Structure. *IEEE Transactions on Electron Devices*, **2007**, 54, 2969-2974	2.9	12
316	Simulation of the effect of parasitic channel height on characteristics of stacked gate-all-around nanosheet FET. *Solid-State Electronics*, **2020**, 164, 107686	1.7	12
315	Dual Functions of V/SiO/AlO/pSi Device as Selector and Memory. *Nanoscale Research Letters*, **2018**, 13, 252	5	12
314	Gradual switching and self-rectifying characteristics of Cu/□GZO/p+-Si RRAM for synaptic device application. *Solid-State Electronics*, **2018**, 150, 60-65	1.7	12
313	SiO2 layer effect on atomic layer deposition Al2O3-based resistive switching memory. *Applied Physics Letters*, **2019**, 114, 182102	3.4	11
312	A Band-Engineered One-Transistor DRAM With Improved Data Retention and Power Efficiency. *IEEE Electron Device Letters*, **2019**, 40, 562-565	4.4	11
311	Memristive and Synaptic Characteristics of Nitride-Based Heterostructures on Si Substrate. *Nanomaterials*, **2020**, 10,	5.4	11
310	Analysis on Program Disturbance in Channel-Stacked NAND Flash Memory With Layer Selection by Multilevel Operation. *IEEE Transactions on Electron Devices*, **2016**, 63, 1041-1046	2.9	11
309	80nm self-aligned complementary I-MOS using double sidewall spacer and elevated drain structure and its applicability to amplifiers with high linearity		11
308	Multilevel switching memristor by compliance current adjustment for off-chip training of neuromorphic system. *Chaos, Solitons and Fractals*, **2021**, 153, 111587	9.3	11
307	Surface Ge-rich p-type SiGe channel tunnel field-effect transistor fabricated by local condensation technique. *Solid-State Electronics*, **2020**, 164, 107701	1.7	11
306	Pulse area dependent gradual resistance switching characteristics of CMOS compatible SiNx-based resistive memory. *Solid-State Electronics*, **2017**, 132, 109-114	1.7	10
305	Implementation of Boolean Logic Functions in Charge Trap Flash for In-Memory Computing. *IEEE Electron Device Letters*, **2019**, 40, 1358-1361	4.4	10
304	Silicon-based field-induced band-to-band tunnelling effect transistor. *IEEE Electron Device Letters*, **2004**, 25, 439-441	4.4	10

303	Performance improvement of scaled-down top-contact OTFTs by two-step-deposition of pentacene. *IEEE Electron Device Letters*, **2005**, 26, 903-905	4.4	10
302	Comparison of the characteristics of semiconductor gas sensors with different transducers fabricated on the same substrate. *Sensors and Actuators B: Chemical*, **2021**, 335, 129661	8.5	10
301	Si-Based FET-Type Synaptic Device With Short-Term and Long-Term Plasticity Using High- $kappa$ Gate-Stack. *IEEE Transactions on Electron Devices*, **2019**, 66, 917-923	2.9	9
300	Demonstration of Fin-Tunnel Field-Effect Transistor with Elevated Drain. *Micromachines*, **2019**, 10,	3.3	9
299	Highly Reliable Inference System of Neural Networks Using Gated Schottky Diodes. *IEEE Journal of the Electron Devices Society*, **2019**, 7, 522-528	2.3	9
298	Design and Optimization of Triple-k Spacer Structure in Two-Stack Nanosheet FET From OFF-State Leakage Perspective. *IEEE Transactions on Electron Devices*, **2020**, 67, 1317-1322	2.9	9
297	A novel fabrication method for co-integrating ISFET with damage-free sensing oxide and threshold voltage-tunable CMOS read-out circuits. *Sensors and Actuators B: Chemical*, **2018**, 260, 627-634	8.5	9
296	A Vertical 4-Bit SONOS Flash Memory and a Unique 3-D Vertical nor Array Structure. *IEEE Nanotechnology Magazine*, **2010**, 9, 70-77	2.6	9
295	Quantum simulation of noise in silicon nanowire transistors with electron-phonon interactions. *Journal of Applied Physics*, **2009**, 105, 023712	2.5	9
294	Dynamic bias temperature instability-like behaviors under Fowler–Nordheim program/erase stress in nanoscale silicon-oxide-nitride-oxide-silicon memories. *Applied Physics Letters*, **2008**, 92, 133508	3.4	9
293	Effects of High-Pressure Annealing on the Low-Frequency Noise Characteristics in Ferroelectric FET. *IEEE Electron Device Letters*, **2022**, 43, 13-16	4.4	9
292	Simulation of Gate-All-Around Tunnel Field-Effect Transistor with an n-Doped Layer. *IEICE Transactions on Electronics*, **2010**, E93-C, 540-545	0.4	9
291	Effects of Process-Induced Defects on Polarization Switching in Ferroelectric Tunneling Junction Memory. *IEEE Electron Device Letters*, **2021**, 42, 323-326	4.4	9
290	Improvement in Self-Heating Characteristic by Incorporating Hetero-Gate-Dielectric in Gate-All-Around MOSFETs. *IEEE Journal of the Electron Devices Society*, **2021**, 9, 36-41	2.3	9
289	High-Density Reconfigurable Devices With Programmable Bottom-Gate Array. *IEEE Electron Device Letters*, **2017**, 38, 564-567	4.4	8
288	Improved multi-level capability in Si3N4-based resistive switching memory using continuous gradual reset switching. *Journal Physics D: Applied Physics*, **2017**, 50, 02LT01	3	8
287	Multi-Level Threshold Voltage Setting Method of String Select Transistors for Layer Selection in Channel Stacked NAND Flash Memory. *IEEE Electron Device Letters*, **2015**, 36, 1318-1320	4.4	8
286	Design and Electrical Characterization of 2-T Thyristor RAM With Low Power Consumption. *IEEE Electron Device Letters*, **2018**, 39, 355-358	4.4	8

285	A Mobility Model for Random Discrete Dopants and Application to the Current Drivability of DRAM Cell. *IEEE Transactions on Electron Devices*, **2017**, 64, 4246-4251	2.9	8
284	Unipolar resistive switching characteristics of W/Si3N4/Si memory devices with doped silicon bottom electrodes. *Current Applied Physics*, **2017**, 17, 146-151	2.6	8
283	A BJT-Based Heterostructure 1T-DRAM for Low-Voltage Operation. *IEEE Electron Device Letters*, **2012**, 33, 14-16	4.4	8
282	Analysis of hysteresis characteristics of silicon nanowire biosensors in aqueous environment. *Applied Physics Letters*, **2011**, 99, 252103	3.4	8
281	LAyer Selection by ERase (LASER) With an Etch-Through-Spacer Technique in a Bit-Line Stacked 3-D nand Flash Memory Array. *IEEE Transactions on Electron Devices*, **2011**, 58, 1892-1897	2.9	8
280	A New Noise Parameter Model of Short-Channel MOSFETs. *Radio Frequency Integrated Circuits (RFIC) Symposium, IEEE*, **2007**,		8
279	Negative-differential transconductance characteristics at room temperature in 30-nm square-channel SOI nMOSFETs with a degenerately doped body. *IEEE Electron Device Letters*, **2002**, 23, 612-614	4.4	8
278	Electrical and Thermal Performances of Omega-Shaped-Gate Nanowire Field Effect Transistors for Low Power Operation. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 4092-4096	1.3	8
277	Realization of Biomimetic Synaptic Functions in a One-Cell Organic Resistive Switching Device Using the Diffusive Parameter of Conductive Filaments. *ACS Applied Materials & Interfaces*, **2020**, 12, 51719-51728	9.5	8
276	Optimization of post-deposition annealing temperature for improved signal-to-noise ratio in In2O3 gas sensor. *Semiconductor Science and Technology*, **2021**, 36, 075007	1.8	8
275	Design and Characterization of Semi-Floating-Gate Synaptic Transistor. *Micromachines*, **2019**, 10,	3.3	8
274	Effect of charge storage engineering on the NO gas sensing properties of a WO FET-type gas sensor with a horizontal floating-gate. *Nanoscale*, **2021**, 13, 9009-9017	7.7	8
273	Space Program Scheme for 3-D NAND Flash Memory Specialized for the TLC Design **2018**,		8
272	GaN-based light emitting diodes using p-type trench structure for improving internal quantum efficiency. *Applied Physics Letters*, **2017**, 110, 021115	3.4	7
271	Fabrication and Characterization of TiOx Memristor for Synaptic Device Application. *IEEE Nanotechnology Magazine*, **2020**, 19, 475-480	2.6	7
270	Investigation of Sidewall High-k Interfacial Layer Effect in Gate-All-Around Structure. *IEEE Transactions on Electron Devices*, **2020**, 67, 1859-1863	2.9	7
269	Elimination of the gate and drain bias stresses in IV characteristics of WSe2 FETs by using dual channel pulse measurement. *Applied Physics Letters*, **2016**, 109, 053503	3.4	7
268	Neuromorphic System Based on CMOS Inverters and Si-Based Synaptic Device. *Journal of Nanoscience and Nanotechnology*, **2016**, 16, 4709-12	1.3	7

267	Unsupervised Online Learning With Multiple Postsynaptic Neurons Based on Spike-Timing-Dependent Plasticity Using a Thin-Film Transistor-Type NOR Flash Memory Array. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6050-6054	1.3	7
266	Overflow Handling Integrate-and-Fire Silicon-on-Insulator Neuron Circuit Incorporating a Schmitt Trigger Implemented by Back-Gate Effect. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6183-6186	1.3	7
265	A Low-Energy High-Density Capacitor-Less I&F Neuron Circuit Using Feedback FET Co-Integrated With CMOS. *IEEE Journal of the Electron Devices Society*, **2019**, 1-1	2.3	7
264	Mixed-Mode Simulation of Nanowire Ge/GaAs Heterojunction Tunneling Field-Effect Transistor for Circuit Applications. *IEEE Journal of the Electron Devices Society*, **2013**, 1, 48-53	2.3	7
263	Observation of Slow Oxide Traps at MOSFETs Having Metal/High-k Gate Dielectric Stack in Accumulation Mode. *IEEE Transactions on Electron Devices*, **2010**, 57, 2697-2703	2.9	7
262	Design and optimization of two-bit double-gate nonvolatile memory cell for highly reliable operation. *IEEE Nanotechnology Magazine*, **2006**, 5, 180-185	2.6	7
261	Analysis of the spurious negative resistance of PN junction avalanche breakdown. *IEEE Transactions on Electron Devices*, **1999**, 46, 230-236	2.9	7
260	A Novel Vector-matrix Multiplication (VMM) Architecture based on NAND Memory Array. *Journal of Semiconductor Technology and Science*, **2020**, 20, 242-248	1.5	7
259	Asymmetric dual-gate-structured one-transistor dynamic random access memory cells for retention characteristics improvement. *Applied Physics Express*, **2016**, 9, 084201	2.4	7
258	Low-power and reliable gas sensing system based on recurrent neural networks. *Sensors and Actuators B: Chemical*, **2021**, 340, 129258	8.5	7
257	Neuromorphic Technology Based on Charge Storage Memory Devices **2018**,		7
256	InGaN/GaN light-emitting diode having direct hole injection plugs and its high-current operation. *Optics Express*, **2017**, 25, 6440-6449	3.3	6
255	Analysis on Reverse Drain-Induced Barrier Lowering and Negative Differential Resistance of Ferroelectric-Gate Field-Effect Transistor Memory. *IEEE Electron Device Letters*, **2020**, 41, 1197-1200	4.4	6
254	Investigation of the Thermal Recovery From Reset Breakdown of a SiNx-Based RRAM. *IEEE Transactions on Electron Devices*, **2020**, 67, 1600-1605	2.9	6
253	Negative Capacitance Effect on MOS Structure: Influence of Electric Field Variation. *IEEE Nanotechnology Magazine*, **2020**, 19, 168-171	2.6	6
252	Impact of the Sub-Resting Membrane Potential on Accurate Inference in Spiking Neural Networks. *Scientific Reports*, **2020**, 10, 3515	4.9	6
251	Vertical-Structured Electron-Hole Bilayer Tunnel Field-Effect Transistor for Extremely Low-Power Operation With High Scalability. *IEEE Transactions on Electron Devices*, **2018**, 65, 2010-2015	2.9	6
250	A novel SiNW/CMOS hybrid biosensor for high sensitivity/low noise **2013**,		6

249	Extraction of Location and Energy Level of the Trap Causing Random Telegraph Noise at Reverse-Biased Region in GaN-Based Light-Emitting Diodes. *IEEE Transactions on Electron Devices*, **2012**, 59, 3495-3502	2.9	6
248	Silicon-compatible bulk-type compound junctionless field-effect transistor **2011**,		6
247	Fabrication and Characteristics of Self-Aligned Dual-Gate Single-Electron Transistors. *IEEE Nanotechnology Magazine*, **2009**, 8, 492-497	2.6	6
246	Physics-Based Analysis and Simulation of $hbox{1}/f$ Noise in MOSFETs Under Large-Signal Operation. *IEEE Transactions on Electron Devices*, **2010**, 57, 1110-1118	2.9	6
245	Twin-bit silicon-oxide-nitride-oxide-silicon (SONOS) memory by inverted sidewall patterning (TSM-ISP). *IEEE Nanotechnology Magazine*, **2003**, 2, 246-252	2.6	6
244	Characterization issues of gate geometry in multifinger structure for RF-SOI MOSFETs. *IEEE Electron Device Letters*, **2002**, 23, 288-290	4.4	6
243	Comprehensive and accurate analysis of the working principle in ferroelectric tunnel junctions using low-frequency noise spectroscopy.. *Nanoscale*, **2022**,	7.7	6
242	Efficient precise weight tuning protocol considering variation of the synaptic devices and target accuracy. *Neurocomputing*, **2020**, 378, 189-196	5.4	6
241	Sensitivity Analysis Based on Neural Network for Optimizing Device Characteristics. *IEEE Electron Device Letters*, **2020**, 41, 1548-1551	4.4	6
240	. *IEEE Access*, **2020**, 8, 202639-202647	3.5	6
239	Nanoscale wedge resistive-switching synaptic device and experimental verification of vector-matrix multiplication for hardware neuromorphic application. *Japanese Journal of Applied Physics*, **2021**, 60, 050905	1.4	6
238	Impacts of Program/Erase Cycling on the Low-Frequency Noise Characteristics of Reconfigurable Gated Schottky Diodes. *IEEE Electron Device Letters*, **2021**, 42, 863-866	4.4	6
237	Analysis on temperature dependent current mechanism of tunnel field-effect transistors. *Japanese Journal of Applied Physics*, **2016**, 55, 06GG03	1.4	6
236	Highly improved response and recovery characteristics of Si FET-type gas sensor using pre-bias **2016**,		6
235	4-bit Multilevel Operation in Overshoot Suppressed Al 2 O 3 /TiO x Resistive Random-Access Memory Crossbar Array. *Advanced Intelligent Systems*,2100273	6	6
234	A Spiking Neural Network with a Global Self-Controller for Unsupervised Learning Based on Spike-Timing-Dependent Plasticity Using Flash Memory Synaptic Devices **2019**,		5
233	Characterization of a Capacitorless DRAM Cell for Cryogenic Memory Applications. *IEEE Electron Device Letters*, **2019**, 40, 1614-1617	4.4	5
232	Partial Isolation Type Saddle-FinFET(Pi-FinFET) for Sub-30 nm DRAM Cell Transistors. *Electronics (Switzerland)*, **2019**, 8, 8	2.6	5

231	Effect of Nitrogen Content in Tunneling Dielectric on Cell Properties of 3-D NAND Flash Cells. *IEEE Electron Device Letters*, **2019**, 40, 702-705	4.4	5
230	Analog Complementary Metal-Oxide-Semiconductor Integrate-and-Fire Neuron Circuit for Overflow Retaining in Hardware Spiking Neural Networks. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 3117-3122	1.3	5
229	Spiking Neural Networks with Unsupervised Learning Based on STDP Using Resistive Synaptic Devices and Analog CMOS Neuron Circuit. *Journal of Nanoscience and Nanotechnology*, **2018**, 18, 6588-6592	1.3	5
228	Theory of 1/f noise currents in semiconductor devices with one-dimensional geometry and its application to Si Schottky barrier diodes. *IEEE Transactions on Electron Devices*, **2001**, 48, 2875-2883	2.9	5
227	Low-frequency noise degradation caused by STI interface effects in SOI-MOSFETs. *IEEE Electron Device Letters*, **2001**, 22, 449-451	4.4	5
226	Surface morphology and I-V characteristics of single-crystal, polycrystalline, and amorphous silicon FEAs. *IEEE Electron Device Letters*, **1999**, 20, 215-218	4.4	5
225	Optimization of channel structure and bias condition for signal-to-noise ratio improvement in Si-based FET-type gas sensor with horizontal floating-gate. *Sensors and Actuators B: Chemical*, **2022**, 357, 131398	8.5	5
224	Study on Threshold Voltage Control of Tunnel Field-Effect Transistors Using VT-Control Doping Region. *IEICE Transactions on Electronics*, **2012**, E95.C, 820-825	0.4	5
223	Ferroelectricity of pure HfOx in metal-ferroelectric-insulator-semiconductor stacks and its memory application. *Applied Surface Science*, **2022**, 573, 151566	6.7	5
222	Vertically Stacked Gate-All-Around Structured Tunneling-Based Ternary-CMOS. *IEEE Transactions on Electron Devices*, **2020**, 67, 3889-3893	2.9	5
221	Input-modulating adaptive neuron circuit employing asymmetric floating-gate MOSFET with two independent control gates. *Solid-State Electronics*, **2020**, 163, 107667	1.7	5
220	Tunneling oxide engineering for improving retention in nonvolatile charge-trapping memory with TaN/Al2O3/HfO2/SiO2/Al2O3/SiO2/Si structure. *Japanese Journal of Applied Physics*, **2020**, 59, 061006	1.4	5
219	Fabrication of asymmetric independent dual-gate FinFET using sidewall spacer patterning and CMP processes. *Microelectronic Engineering*, **2018**, 185-186, 29-34	2.5	5
218	A Si FET-type Gas Sensor with Pulse-driven Localized Micro-heater for Low Power Consumption **2018**,		5
217	Near-Linear Potentiation Mechanism of Gated Schottky Diode as a Synaptic Device. *IEEE Journal of the Electron Devices Society*, **2019**, 7, 335-343	2.3	4
216	An Analysis of Hole Trapping at Grain Boundary or Poly-Si Floating-Body MOSFET. *Journal of Nanoscience and Nanotechnology*, **2018**, 18, 6584-6587	1.3	4
215	Fabrication of n-Type CNT Field-Effect Transistor Using Energy Band Engineering Layer Between CNT and Electrode. *IEEE Electron Device Letters*, **2013**, 34, 1436-1438	4.4	4
214	High-Density Three-Dimensional Stacked nand Flash With Common Gate Structure and Shield Layer. *IEEE Transactions on Electron Devices*, **2011**, 58, 4212-4218	2.9	4

213	Quantum simulation of noise in silicon nanowire transistors. *Journal of Applied Physics*, **2008**, 104, 023708	2.5	4
212	Stable extraction of linearity (V/sub IP3/) for nanoscale RF CMOS devices. *IEEE Microwave and Wireless Components Letters*, **2004**, 14, 83-85	2.6	4
211	Realistic single-electron transistor modeling and novel CMOS/SET hybrid circuits		4
210	SiO2 Fin-Based Flash Synaptic Cells in AND Array Architecture for Binary Neural Networks. *IEEE Electron Device Letters*, **2022**, 43, 142-145	4.4	4
209	Field Effect Transistor-Type Devices Using High-□Gate Insulator Stacks for Neuromorphic Applications. *ACS Applied Electronic Materials*, **2020**, 2, 323-328	4	4
208	3D Integrable W/SiN/n-Si/p-Si 1D1R Unipolar Resistive Random Access Memory Synapse for Suppressing Reverse Leakage in Spiking Neural Network. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 4735-4739	1.3	4
207	Multilevel Switching Characteristics of Si3N4-Based Nano-Wedge Resistive Switching Memory and Array Simulation for In-Memory Computing Application. *Electronics (Switzerland)*, **2020**, 9, 1228	2.6	4
206	. *IEEE Transactions on Electron Devices*, **2020**, 67, 4541-4544	2.9	4
205	Investigation of Low-Frequency Noise Characteristics in Gated Schottky Diodes. *IEEE Electron Device Letters*, **2021**, 42, 442-445	4.4	4
204	Improvement of self-heating effect in Ge vertically stacked GAA nanowire pMOSFET by utilizing Al2O3 for high-performance logic device and electrical/thermal co-design. *Japanese Journal of Applied Physics*, **2021**, 60, SCCE04	1.4	4
203	Physical Unclonable Functions Using Ferroelectric Tunnel Junctions. *IEEE Electron Device Letters*, **2021**, 42, 816-819	4.4	4
202	Hardware-Based Spiking Neural Network Using a TFT-Type AND Flash Memory Array Architecture Based on Direct Feedback Alignment. *IEEE Access*, **2021**, 9, 73121-73132	3.5	4
201	Interlayer engineering for enhanced ferroelectric tunnel junction operations in HfO-based metal-ferroelectric-insulator-semiconductor stack. *Nanotechnology*, **2021**, 32,	3.4	4
200	Efficient fusion of spiking neural networks and FET-type gas sensors for a fast and reliable artificial olfactory system. *Sensors and Actuators B: Chemical*, **2021**, 345, 130419	8.5	4
199	Investigation of Low-Frequency Noise Characteristics of Ferroelectric Tunnel Junction: from Conduction Mechanism and Scaling Perspectives. *IEEE Electron Device Letters*, **2022**, 1-1	4.4	4
198	An Analytical Model for the Threshold Voltage of Intrinsic Channel MOSFET Having Bulk Trap Charges. *IEEE Transactions on Electron Devices*, **2017**, 64, 2113-2120	2.9	3
197	Synaptic device using a floating fin-body MOSFET with memory functionality for neural network. *Solid-State Electronics*, **2019**, 156, 23-27	1.7	3
196	Trap Profiling in Nitride Storage Layer in 3-D NAND Flash Memory Using Retention Characteristics and AC- $text{g}_{mathrm {m}}$ Method. *IEEE Electron Device Letters*, **2015**, 36, 561-563	4.4	3

195	Vertical Inner Gate Transistors for 4F2 DRAM Cell. *IEEE Transactions on Electron Devices*, **2020**, 67, 944-948	2.9	3
194	Extension of the DG Model to the Second-Order Quantum Correction for Analysis of the Single-Charge Effect in Sub-10-nm MOS Devices. *IEEE Journal of the Electron Devices Society*, **2020**, 1-1	2.3	3
193	Novel Boosting Scheme Using Asymmetric Pass Voltage for Reducing Program Disturbance in 3-Dimensional NAND Flash Memory. *IEEE Journal of the Electron Devices Society*, **2018**, 1-1	2.3	3
192	Investigation of silicide-induced-dopant-activation for steep tunnel junction in tunnel field effect transistor (TFET). *Solid-State Electronics*, **2018**, 140, 41-45	1.7	3
191	A 1T-DRAM cell based on a tunnel field-effect transistor with highly-scalable pillar and surrounding gate structure. *Journal of the Korean Physical Society*, **2016**, 69, 323-327	0.6	3
190	Layer Selection by Multi-Level Permutation in 3-D Stacked NAND Flash Memory. *IEEE Electron Device Letters*, **2016**, 37, 866-869	4.4	3
189	Analysis on New Read Disturbance Induced by Hot Carrier Injections in 3-D Channel-Stacked NAND Flash Memory. *IEEE Transactions on Electron Devices*, **2019**, 66, 3326-3330	2.9	3
188	Investigation of Sensor Performance in Accumulation- and Inversion-Mode Silicon Nanowire pH Sensors. *IEEE Transactions on Electron Devices*, **2014**, 61, 1607-1610	2.9	3
187	Investigation on multiple activation energy of retention in charge trapping memory using self-consistent simulation **2014**,		3
186	Flicker Noise Behavior in Resistive Memory Devices With Double-Layered Transition Metal Oxide. *IEEE Electron Device Letters*, **2013**, 34, 244-246	4.4	3
185	Understanding Reset Transitions in Ni/SiNx/Si Resistive Random-Access Memory. *Journal of Nanoscience and Nanotechnology*, **2017**, 17, 7231-7235	1.3	3
184	Improved internal quantum efficiency of GaN-based light emitting diodes using p-AlGaN trench in multi-quantum well. *Japanese Journal of Applied Physics*, **2014**, 53, 06JE14	1.4	3
183	Carbon Nanotube-Based CMOS Gas Sensor IC: Monolithic Integration of Pd Decorated Carbon Nanotube Network on a CMOS Chip and Its Hydrogen Sensing. *IEEE Transactions on Electron Devices* , **2011**, 58, 3604-3608	2.9	3
182	A 2-Bit Recessed Channel Nonvolatile Memory Device With a Lifted Charge-Trapping Node. *IEEE Nanotechnology Magazine*, **2009**, 8, 111-115	2.6	3
181	Accurate extraction of D_{it} due to random telegraph noise in gate edge current of high-k n-type metal-oxide-semiconductor field-effect transistors under accumulation mode. *Applied Physics Letters*, **2011**, 98, 023505	3.4	3
180	Statistical property of the effect of Au nanoparticle decoration on the carbon nanotube network. *Applied Physics Letters*, **2011**, 98, 143106	3.4	3
179	Channel doping concentration and fin width effects on self-boosting in NAND-type SONOS flash memory array based on bulk-FinFETs **2009**,		3
178	A capacitor-less 1T-DRAM cell with vertical surrounding gates using gate-induced drain-leakage (GIDL) current **2008**,		3

177	Depletion-enhanced body-isolation (DEBI) array on SOI for highly scalable and reliable NAND flash memories. *IEEE Nanotechnology Magazine*, **2006**, 5, 201-204	2.6	3
176	Improving the Endurance Characteristics Through Boron Implant at Active Edge in 1 G NAND Flash **2007**,		3
175	Complementary self-biased scheme for the robust design of CMOS/SET hybrid multi-valued logic		3
174	Reverse-order source/drain formation with double offset spacer (RODOS) for low-power and high-speed application. *IEEE Nanotechnology Magazine*, **2003**, 2, 210-216	2.6	3
173	Effects of Channel Length Scaling on the Signal-to-Noise Ratio in FET-Type Gas sensor with Horizontal Floating-Gate. *IEEE Electron Device Letters*, **2022**, 1-1	4.4	3
172	Capacitor-Based Synaptic Devices for Hardware Spiking Neural Networks. *IEEE Electron Device Letters*, **2022**, 1-1	4.4	3
171	Insertion of Ag Layer in TiN/SiNx/TiN RRAM and Its Effect on Filament Formation Modeled by Monte Carlo Simulation. *IEEE Access*, **2020**, 8, 228720-228730	3.5	3
170	Implementation of Synaptic Device Using Various High- Gate Dielectric Stacks. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 4292-4297	1.3	3
169	Suppression of reverse drain induced barrier lowering in negative capacitance FDSOI field effect transistor using oxide charge trapping layer. *Semiconductor Science and Technology*, **2020**, 35, 125003	1.8	3
168	Solving Overlapping Pattern Issues in On-Chip Learning of Bio-Inspired Neuromorphic System with Synaptic Transistors. *Electronics (Switzerland)*, **2020**, 9, 13	2.6	3
167	A Quantum-Well Charge-Trap Synaptic Transistor With Highly Linear Weight Tunability. *IEEE Journal of the Electron Devices Society*, **2020**, 8, 834-840	2.3	3
166	Bias Polarity Dependent Resistive Switching Behaviors in Silicon Nitride-Based Memory Cell. *IEICE Transactions on Electronics*, **2016**, E99.C, 547-550	0.4	3
165	Back biasing effects in a feedback steep switching device with charge spacer **2016**,		3
164	Investigation on Ambipolar Current Suppression Using a Stacked Gate in an L-shaped Tunnel Field-Effect Transistor. *Micromachines*, **2019**, 10,	3.3	3
163	Ni/GeOx/p+ Si resistive-switching random-access memory with full Si processing compatibility and its characterization and modeling. *Vacuum*, **2019**, 161, 63-70	3.7	3
162	Investigation of transient current characteristics with scaling-down poly-Si body thickness and grain size of 3D NAND flash memory. *Solid-State Electronics*, **2019**, 152, 41-45	1.7	3
161	Trap-Induced Data-Retention-Time Degradation of DRAM and Improvement Using Dual Work-Function Metal Gate. *IEEE Electron Device Letters*, **2021**, 42, 38-41	4.4	3
160	Circuit-level simulation of resistive-switching random-access memory cross-point array based on a highly reliable compact model. *Journal of Computational Electronics*, **2018**, 17, 273-278	1.8	3

159	Concurrent events of memory and threshold switching in Ag/SiNx/Si devices. *Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics*, **2018**, 36, 051203	1.3	3
158	3-D AND-Type Flash Memory Architecture With High-□Gate Dielectric for High-Density Synaptic Devices. *IEEE Transactions on Electron Devices*, **2021**, 68, 3801-3806	2.9	3
157	A More Hardware-Oriented Spiking Neural Network Based on Leading Memory Technology and Its Application With Reinforcement Learning. *IEEE Transactions on Electron Devices*, **2021**, 68, 4411-4417	2.9	3
156	Effects of Postdeposition Annealing Ambience on NO□Gas Sensing Performance in Si-Based FET-Type Gas Sensor. *IEEE Transactions on Electron Devices*, **2022**, 1-7	2.9	3
155	Comparison of writing methods of single memory cell with volatile and nonvolatile memory functions. *Applied Physics Express*, **2017**, 10, 064201	2.4	2
154	Analysis of Clockwise and Counter-Clockwise Hysteresis Characteristics in 3-D NAND Flash Memory Cells. *IEEE Electron Device Letters*, **2017**, 38, 867-870	4.4	2
153	Oxide Thin Film Transistor With a Novel Gate Insulator Stack to Suppress Photo-Excited Charge Injection. *IEEE Nanotechnology Magazine*, **2019**, 18, 491-493	2.6	2
152	Resistive random-access memory with an a-Si/SiNx double-layer. *Solid-State Electronics*, **2019**, 158, 64-69	1.7	2
151	Effect of Word-Line Bias on Linearity of Multi-Level Conductance Steps for Multi-Layer Neural Networks Based on NAND Flash Cells. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 4138-4142	1.3	2
150	HfO x -based nano-wedge structured resistive switching memory device operating at sub-□A current for neuromorphic computing application. *Semiconductor Science and Technology*, **2020**, 35, 055002	1.8	2
149	Design Consideration of Diode-Type NAND Flash Memory Cell String Having Super-Steep Switching Slope. *IEEE Journal of the Electron Devices Society*, **2016**, 4, 328-334	2.3	2
148	Near-Infrared Detection Using Pulsed Tunneling Junction in Silicon Devices. *IEEE Transactions on Electron Devices*, **2016**, 63, 377-383	2.9	2
147	Reconfigurable Cell String Having FET and Super-Steep Switching Diode Operation in 3D NAND Flash Memory **2018**,		2
146	A new device characteristic model generation by machine learning **2019**,		2
145	Tunnel Field Effect Transistor with Ferroelectric Gate Insulator. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6095-6098	1.3	2
144	Grayscale Image Recognition Using Spike-Rate-Based Online Learning and Threshold Adjustment of Neurons in a Thin-Film Transistor-Type NOR Flash Memory Array. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6055-6060	1.3	2
143	A systematic model parameter extraction using differential evolution searching **2019**,		2
142	Switching and conduction mechanism of Cu/Si3N4/Si RRAM with CMOS compatibility **2014**,		2

141	Simulation study on scaling limit of silicon tunneling field-effect transistor under tunneling-predominance. *IEICE Electronics Express*, **2012**, 9, 828-833	0.5	2
140	Investigation on hump effects of L-shaped tunneling filed-effect transistors **2012**,		2
139	Characteristics of Elliptical Gate-All-Around SONOS Nanowire With Effective Circular Radius. *IEEE Electron Device Letters*, **2012**, 33, 1613-1615	4.4	2
138	Electrical instabilities and low-frequency noise in InGaZnO thin film transistors **2010**,		2
137	A Simple compact model for hot carrier injection phenomenon in 32 nm NAND flash memory device **2010**,		2
136	Experimental Investigation of Quasi-Ballistic Carrier Transport Characteristics in 10-nm Scale MOSFETs. *IEEE Nanotechnology Magazine*, **2011**, 10, 975-979	2.6	2
135	Body-raised double-gate structure for 1T DRAM **2009**,		2
134	Stacked Gated Twin-Bit (SGTB) SONOS Memory Device for High-Density Flash Memory. *IEEE Nanotechnology Magazine*, **2012**, 11, 307-313	2.6	2
133	Analytical modeling of field-induced interband tunneling-effect transistors and its application. *IEEE Nanotechnology Magazine*, **2006**, 5, 192-200	2.6	2
132	Pattern multiplication method and the uniformity of nanoscale multiple lines. *Journal of Vacuum Science & Technology an Official Journal of the American Vacuum Society B, Microelectronics Processing and Phenomena*, **2003**, 21, 1491		2
131	Coulomb oscillations based on band-to-band tunneling in a degenerately doped silicon metal-oxide-semiconductor field-effect transistor. *Applied Physics Letters*, **2004**, 84, 3178-3180	3.4	2
130	Simulation of Ion Conduction in the ompF Porin Channel Using BioMOCA. *Journal of Computational Electronics*, **2005**, 4, 157-160	1.8	2
129	SOI MOSFET structure with a junction-type body contact for suppression of pass gate leakage. *IEEE Transactions on Electron Devices*, **2001**, 48, 1360-1365	2.9	2
128	A formation of cobalt silicide on silicon field emitter arrays by electrical stress. *IEEE Electron Device Letters*, **2001**, 22, 173-175	4.4	2
127	Mo and Co Silicide FEAs. *Materials Research Society Symposia Proceedings*, **2000**, 621, 411		2
126	Threshold voltage reduction model for buried channel PMOSFETs using quasi-2-D Poisson equation. *IEEE Transactions on Electron Devices*, **2000**, 47, 2326-2333	2.9	2
125	An anomalous device degradation of SOI devices with STI		2
124	A leakage current mechanism caused by the interaction of residual oxidation stress and high-energy ion implantation impact in advanced CMOS technology. *IEEE Electron Device Letters*, **1999**, 20, 251-253	4.4	2

123	Programming dynamics of a single electron memory cell with a high-density SiGe nanocrystal array at room temperature		2
122	Comparative Study on Top- and Bottom-Source Vertical-Channel Tunnel Field-Effect Transistors. *IEICE Transactions on Electronics*, **2012**, E95.C, 826-830	0.4	2
121	Investigation on Tunneling-based Ternary CMOS with Ferroelectric-Gate Field Effect Transistor Using TCAD Simulation. *Applied Sciences (Switzerland)*, **2020**, 10, 4977	2.6	2
120	3D AND-Type Stacked Array for Neuromorphic Systems. *Micromachines*, **2020**, 11,	3.3	2
119	Effect of Ag source layer thickness on the switching mechanism of TiN/Ag/SiN x /TiN conductive bridging random access memory observed at sub-□A current. *Semiconductor Science and Technology* , **2021**, 36, 055014	1.8	2
118	Synaptic Device With High Rectification Ratio Resistive Switching and Its Impact on Spiking Neural Network. *IEEE Transactions on Electron Devices*, **2021**, 68, 1610-1615	2.9	2
117	Multiplexed Silicon Nanowire Tunnel FET-Based Biosensors With Optimized Multi-Sensing Currents. *IEEE Sensors Journal*, **2021**, 21, 8839-8846	4	2
116	Novel Program Method of String Select Transistors for Layer Selection in Channel-Stacked NAND Flash Memory. *IEEE Transactions on Electron Devices*, **2016**, 63, 3521-3526	2.9	2
115	A Pseudobipolar Junction Transistor for a Sensitive Optical Detection of Biomolecules. *IEEE Transactions on Electron Devices*, **2016**, 63, 2074-2079	2.9	2
114	Hardware-based spiking neural network architecture using simplified backpropagation algorithm and homeostasis functionality. *Neurocomputing*, **2021**, 428, 153-165	5.4	2
113	Spiking Neural Networks With Time-to-First-Spike Coding Using TFT-Type Synaptic Device Model. *IEEE Access*, **2021**, 9, 78098-78107	3.5	2
112	Simulation Analysis in Sub-0.1 □m for Partial Isolation Field-Effect Transistors. *Electronics (Switzerland)*, **2018**, 7, 227	2.6	2
111	A novel physical unclonable function (PUF) using 16□□16 pure-HfOferroelectric tunnel junction array for security applications. *Nanotechnology*, **2021**, 32,	3.4	2
110	Vertically-Stacked Si0.2Ge0.8 Nanosheet Tunnel FET With 70 mV/Dec Average Subthreshold Swing. *IEEE Electron Device Letters*, **2021**, 1-1	4.4	2
109	Effect of weight overlap region on neuromorphic system with memristive synaptic devices. *Chaos, Solitons and Fractals*, **2022**, 157, 111999	9.3	2
108	Effect of Program Error in Memristive Neural Network With Weight Quantization. *IEEE Transactions on Electron Devices*, **2022**, 1-7	2.9	2
107	Fully integrated FET-type gas sensor with optimized signal-to-noise ratio for H2S gas detection. *Sensors and Actuators B: Chemical*, **2022**, 367, 132052	8.5	2
106	The Effect of Drain Bias Stress on the Instability of Turned-OFF Amorphous HfInZnO Thin-Film Transistors Under Light Irradiation. *IEEE Transactions on Electron Devices*, **2017**, 64, 153-158	2.9	1

105	Analysis of Hot Carrier Injection According to Gate Length. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6746-6749	1.3	1
104	Analysis of Minority Carrier Lifetime Dependence on Dual Gate Feedback Field Effect Transistor. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6767-6770	1.3	1
103	Novel Fabrication Method for Forming Damage-Free Sensing Oxide and Threshold Voltage-Tunable Complementary Metal-Oxide Semiconductor in a pH Sensor-CMOS Hybrid System. *Journal of Nanoscience and Nanotechnology*, **2017**, 17, 8265-8270	1.3	1
102	Featuring of transient tunneling current by voltage pulse and application to an electrochemical biosensor. *Journal of Applied Physics*, **2018**, 123, 124902	2.5	1
101	Channel-Stacked NAND Flash Memory With Tied Bit-Line and Ground Select Transistor. *IEEE Electron Device Letters*, **2016**, 37, 1418-1421	4.4	1
100	Volatile and Nonvolatile Characteristics of Asymmetric Dual-Gate Thyristor RAM with Vertical Structure. *Journal of Nanoscience and Nanotechnology*, **2018**, 18, 5882-5886	1.3	1
99	Reversible nonvolatile and threshold switching characteristics in Cu/high-k/Si devices. *IEICE Electronics Express*, **2019**, 16, 20190404-20190404	0.5	1
98	Polysilicon-Based Synaptic Transistor and Array Structure for Short/Long-Term Memory. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6066-6069	1.3	1
97	Transient Analysis of Tunnel Field-Effect Transistor with Raised Drain. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6212-6216	1.3	1
96	An Online Learning Method Using Spike-Timing Dependent Plasticity for Neuromorphic Systems. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6776-6780	1.3	1
95	Silicon Tunneling Field Effect Transistors with a Hemicylindrical Nanowire Channel for Ultra-Low Power Application **2014**,		1
94	Extraction of Interface Trap Density in the Region Between Adjacent Wordlines in NAND Flash Memory Strings. *IEEE Electron Device Letters*, **2015**, 36, 53-55	4.4	1
93	Universal relaxation characteristic of interface trap under FN and NBTI stress in pMOSFET device. *Electronics Letters*, **2014**, 50, 1877-1879	1.1	1
92	Design improvement of L-shaped tunneling field-effect transistors **2012**,		1
91	63.4: Extraction of the Location and the Energy Level of the Trap using Random Telegraph Noise in GaN-based Light-Emitting Diode. *Digest of Technical Papers SID International Symposium*, **2012**, 43, 865-868	0.5	1
90	Poly-silicon quantum-dot single-electron transistors. *Journal of the Korean Physical Society*, **2012**, 60, 108-112	0.6	1
89	L-Shaped Tunneling Field-Effect Transistors for Complementary Logic Applications. *IEICE Transactions on Electronics*, **2013**, E96.C, 634-638	0.4	1
88	Novel MOSFET structure using p-n junction gate for ultra-low subthreshold-swing **2011**,		1

87	Compact modeling of silicon nanowire MOSFET for radio frequency applications. *Microwave and Optical Technology Letters*, **2011**, 53, 471-473	1.2	1
86	Effects of aluminum layer and oxidation on TiO2 based bipolar resistive random access memory (RRAM) **2010**,		1
85	Investigation of 1T DRAM cell with non-overlap structure and recessed channel **2010**,		1
84	Irregular resistive switching characteristics and its mechanism based on NiO unipolar switching resistive random access memory (RRAM) **2010**,		1
83	A comparative study of the program efficiency of gate all around SONOS and TANOS flash memory **2010**,		1
82	A 3-D Statistical Simulation Study of Mobility Fluctuations in MOSFET Induced by Discrete Trapped Charges in SiO $_2$ Layer. *IEEE Nanotechnology Magazine*, **2011**, 10, 699-705	2.6	1
81	Simulation study for suppressing corner effect in a saddle MOSFET for Sub-50 nm high density high performance DRAM cell transistor **2009**,		1
80	Non-ideal characteristic analysis of GaN-based light-emitting diode using current-voltage (IV) and low-frequency noise experiment **2011**,		1
79	Cathodo- and electro- luminescences image mapping technique to study traps in GaN-based LEDs **2012**,		1
78	Simulation of self gating effect of a liquid gate carbon nanotube field effect transistor **2008**,		1
77	Breakdown voltage reduction in I-MOS devices **2006**,		1
76	Vertical AND (V-AND) array: High density, high speed, and reliable flash array **2007**,		1
75	Reliability Studies on Non Planar DRAM Cell Transistor **2007**,		1
74	A novel gated transmission line method for organic thin film transistors **2007**,		1
73	Poly-silicon quantum dot single electron transistors **2007**,		1
72	Fin width variation effects on program disturbance characteristics in a NAND type bulk fin SONOS flash memory **2007**,		1
71	P-18: Performance Improvement of Scaled-down Top-contact OTFTs by Two-Step-Deposition of Pentacene. *Digest of Technical Papers SID International Symposium*, **2005**, 36, 292	0.5	1
70	A dual body SOI structure for mixed analog-digital mode circuits. *IEEE Transactions on Electron Devices*, **2000**, 47, 1617-1623	2.9	1

69	Simple frequency-domain analysis of MOSFET-including nonquasi-static effect. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2001**, 20, 867-876	2.5	1
68	A new SOI MOSFET structure with junction type body contact		1
67	A simple voltage scaling formula for low-power CMOS circuits. *IEEE Transactions on Electron Devices* , **1999**, 46, 803-805	2.9	1
66	Impact of interlayer insulator formation methods on HfOx ferroelectricity in the metalferroelectricInsulatorSemiconductor stack. *Applied Physics Letters*, **2022**, 120, 012901	3.4	1
65	Variation-tolerant Capacitive Array for Binarized Neural Network. *IEEE Electron Device Letters*, **2022** , 1-1	4.4	1
64	Recessed Channel Dual Gate Single Electron Transistors (RCDG-SETs) for Room Temperature Operation. *IEICE Transactions on Electronics*, **2009**, E92-C, 647-652	0.4	1
63	3-Dimensional Terraced NAND (3D TNAND) Flash Memory-Stacked Version of Folded NAND Array. *IEICE Transactions on Electronics*, **2009**, E92-C, 653-658	0.4	1
62	Novel Tunneling Field-Effect Transistor with Sigma-Shape Embedded SiGe Sources and Recessed Channel. *IEICE Transactions on Electronics*, **2013**, E96.C, 639-643	0.4	1
61	Novel Three Dimensional (3D) NAND Flash Memory Array Having Tied Bit-line and Ground Select Transistor (TiGer). *IEICE Transactions on Electronics*, **2012**, E95.C, 837-841	0.4	1
60	Pruning for Hardware-Based Deep Spiking Neural Networks Using Gated Schottky Diode as Synaptic Devices. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 6603-6608	1.3	1
59	A Systematic Compact Model Parameter Calibration with Adaptive Pattern Search Algorithm. *Applied Sciences (Switzerland)*, **2021**, 11, 4155	2.6	1
58	Novel Method Enabling Forward and Backward Propagations in NAND Flash Memory for On-Chip Learning. *IEEE Transactions on Electron Devices*, **2021**, 68, 3365-3370	2.9	1
57	Quantized Weight Transfer Method Using Spike-Timing-Dependent Plasticity for Hardware Spiking Neural Network. *Applied Sciences (Switzerland)*, **2021**, 11, 2059	2.6	1
56	On-chip trainable hardware-based deep Q-networks approximating a backpropagation algorithm. *Neural Computing and Applications*, **2021**, 33, 9391-9402	4.8	1
55	Improvement of Resistive Switching Characteristics of Titanium Oxide Based Nanowedge RRAM Through Nickel Silicidation. *IEEE Transactions on Electron Devices*, **2021**, 68, 438-442	2.9	1
54	Core-Shell Dual-Gate Nanowire Memory as a Synaptic Device for Neuromorphic Application. *IEEE Journal of the Electron Devices Society*, **2021**, 1-1	2.3	1
53	Investigation of Device Performance for Fin Angle Optimization in FinFET and Gate-All-Around FETs for 3 nm-Node and Beyond. *IEEE Transactions on Electron Devices*, **2022**, 69, 2088-2093	2.9	1
52	Highly Efficient Self-Curing Method in MOSFET Using Parasitic Bipolar Junction Transistor. *IEEE Electron Device Letters*, **2022**, 1-1	4.4	1

51	Simulation Program with Integrated Circuit Emphasis Compact Modeling of a Dual-Gate Positive-Feedback Field-Effect Transistor for Circuit Simulations. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6417-6421	1.3	0
50	A theoretical study on tunneling based biosensor having a redox-active monolayer using physics based simulation. *Journal of Applied Physics*, **2018**, 123, 024509	2.5	0
49	A charge pumping device with a potential barrier using inversion charge transfer. *IEEE Transactions on Electron Devices*, **2001**, 48, 1216-1221	2.9	0
48	Comprehensive TCAD-Based Validation of Interface Trap-Assisted Ferroelectric Polarization in Ferroelectric-Gate Field-Effect Transistor Memory. *IEEE Transactions on Electron Devices*, **2022**, 1-6	2.9	0
47	Low-Power Adaptive Integrate-and-Fire Neuron Circuit Using Positive Feedback FET Co-Integrated With CMOS. *IEEE Access*, **2021**, 1-1	3.5	0
46	Ferroelectric-Metal Field-Effect Transistor with Recessed Channel for 1T-DRAM Application. *IEEE Journal of the Electron Devices Society*, **2021**, 1-1	2.3	0
45	Simulation of Retention Characteristics in Double-Gate Structure Multi-Bit SONOS Flash Memory. *IEICE Transactions on Electronics*, **2009**, E92-C, 659-663	0.4	0
44	Double-Gated Ferroelectric-Gate Field-Effect-Transistor for Processing in Memory. *IEEE Electron Device Letters*, **2021**, 1-1	4.4	0
43	Improved rectification characteristics by engineering energy barrier height in TiOx-based RRAM. *Microelectronic Engineering*, **2021**, 237, 111498	2.5	0
42	Selected Bit-Line Current PUF: Implementation of Hardware Security Primitive Based on a Memristor Crossbar Array. *IEEE Access*, **2021**, 9, 120901-120910	3.5	0
41	Effect of Random Dopant Fluctuation on Data Retention Time Distribution in DRAM. *IEEE Transactions on Electron Devices*, **2021**, 1-6	2.9	0
40	Low-Latency Spiking Neural Networks Using Pre-Charged Membrane Potential and Delayed Evaluation. *Frontiers in Neuroscience*, **2021**, 15, 629000	5.1	0
39	Response Comparison of Resistor- and Si FET-Type Gas Sensors on the Same Substrate. *IEEE Transactions on Electron Devices*, **2021**, 68, 3552-3557	2.9	0
38	Direct Gradient Calculation: Simple and Variation-Tolerant On-Chip Training Method for Neural Networks. *Advanced Intelligent Systems*, **2021**, 3, 2100064	6	0
37	Effect of Lateral Charge Diffusion on Retention Characteristics of 3D NAND Flash Cells. *IEEE Electron Device Letters*, **2021**, 42, 1148-1151	4.4	0
36	Gate-First Negative Capacitance Field-Effect Transistor With Self-Aligned Nickel-Silicide Source and Drain. *IEEE Transactions on Electron Devices*, **2021**, 68, 4754-4757	2.9	0
35	On-chip adaptive matching learning with charge-trap synapse device and ReLU activation circuit. *Solid-State Electronics*, **2021**, 186, 108177	1.7	0
34	A Fast Weight Transfer Method for Real-Time Online Learning in RRAM-Based Neuromorphic System. *IEEE Access*, **2022**, 1-1	3.5	0

33	Combination of volatile and non-volatile functions in a single memory cell and its scalability. *Japanese Journal of Applied Physics*, **2017**, 56, 04CE06	1.4
32	Nonvolatile Memory (NVM) Operation of Tunnel Field-Effect Transistor (TFET) Using Ferroelectric HfO□ Sidewall. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6061-6065	1.3
31	Partial Contact Etching and Gate Lowering on Tunneling Field Effect Transistor for Performance and Power Enhancement. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6808-6811	1.3
30	Method to Eliminate Gate and Drain Bias Stresses in Transfer Curves of WSe2 Field Effect Transistors with Single Channel Pulsed I□V Measurement. *Journal of Nanoscience and Nanotechnology*, **2017**, 17, 3382-3385	1.3
29	New Type of Ion-Sensitive Field-Effect Transistor with Sensing Region Separate from Gate-Controlled Region. *Journal of Nanoscience and Nanotechnology*, **2017**, 17, 8280-8284	1.3
28	Detection of Hot Carrier Generated Phonon Using the Gate-Induced Drain Leakage in the Silicon Chip. *IEEE Transactions on Electron Devices*, **2018**, 65, 3915-3921	2.9
27	Vertical stack array of one-time programmable nonvolatile memory based on pn-junction diode and its operation scheme for faster access. *IEICE Electronics Express*, **2014**, 11, 20131041-20131041	0.5
26	Analysis of the internal quantum efficiency of gallium-nitride-based light-emitting diodes from the transient electro-luminescence characteristics. *Journal of the Korean Physical Society*, **2013**, 63, 1186-1188	0.6
25	Metal nanolayer formed by tunnelling current through thin oxide in the electrolyte□oxide□silicon system. *Journal of Experimental Nanoscience*, **2014**, 9, 906-912	1.9
24	A New 1T DRAM Cell: Cone Type 1T DRAM Cell. *IEICE Transactions on Electronics*, **2011**, E94-C, 681-685	0.4
23	Scaling behaviors of silicon-nitride layer for charge-trapping memory. *Journal of Vacuum Science and Technology A: Vacuum, Surfaces and Films*, **2010**, 28, 675-678	2.9
22	Low power size-efficient CMOS UWB low-noise amplifier design. *Microwave and Optical Technology Letters*, **2009**, 51, 494-496	1.2
21	Size efficient low-noise amplifier for 2.4 GHz ISM-band transceiver. *Microwave and Optical Technology Letters*, **2009**, 51, 2304-2308	1.2
20	A Simulation Study on Reducing the Grain Boundary Position Dependency in Tunneling Thin-Film Transistors Using a Wide Tunneling Area. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 6627-6631	1.3
19	I-Shaped SiGe Fin Tunnel Field-Effect Transistor with High / Ratio. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 4298-4302	1.3
18	Detection of Thermal Transport on Chip Using Gate-Induced Drain Leakage Current. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 4980-4984	1.3
17	Utilization of Unsigned Inputs for NAND Flash-Based Parallel and High-Density Synaptic Architecture in Binary Neural Networks. *IEEE Journal of the Electron Devices Society*, **2021**, 1-1	2.3
16	Threshold Voltage Setting Method for Layer Selection by Multi-Level Operation in Channel Stacked NAND Flash Memory. *Journal of Nanoscience and Nanotechnology*, **2017**, 17, 3386-3389	1.3

15	Design and Analysis for 3D Vertical Resistive Random Access Memory Structures with Silicon Bottom Electrodes. *Journal of Nanoscience and Nanotechnology*, **2017**, 17, 7160-7163	1.3
14	Simulation Study on Dependence of Channel Potential Self-Boosting on Device Scale and Doping Concentration in 2-D and 3-D NAND-Type Flash Memory Devices. *IEICE Transactions on Electronics*, **2010**, E93-C, 596-601	0.4
13	Effects of Conductive Defects on Unipolar RRAM for the Improvement of Resistive Switching Characteristics. *IEICE Transactions on Electronics*, **2012**, E95.C, 842-846	0.4
12	New Multiple-Times Programmable CMOS ROM Cell. *IEICE Transactions on Electronics*, **2012**, E95.C, 1098-1103	0.4
11	More physical understanding of current characteristics of tunneling field-effect transistor leveraged by gate positions and properties through dual-gate and gate-all-around structuring. *Applied Physics A: Materials Science and Processing*, **2020**, 126, 1	2.6
10	Analysis of a Schottky Barrier MOSFET for Synaptic Device Using Hot Carrier Injection. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 6592-6595	1.3
9	Double-Gated Asymmetric Floating-Gate-Based Synaptic Device for Effective Performance Enhancement Through Online Learning. *IEEE Access*, **2020**, 8, 217735-217743	3.5
8	Variability of DRAM Peripheral Transistor at Liquid Nitrogen Temperature. *IEEE Transactions on Electron Devices*, **2021**, 68, 1627-1632	2.9
7	Integrate-and-Fire Neuron Circuit With Synaptic Off-Current Blocking Operation. *IEEE Access*, **2021**, 9, 127841-127851	3.5
6	Suppression of Statistical Variability in Stacked Nanosheet Using Floating Fin Structure. *IEEE Electron Device Letters*, **2021**, 1-1	4.4
5	Hardware-Based Spiking Neural Networks Using Capacitor-Less Positive Feedback Neuron Devices. *IEEE Transactions on Electron Devices*, **2021**, 68, 4766-4772	2.9
4	On-Chip Trainable Spiking Neural Networks Using Time-To-First-Spike Encoding. *IEEE Access*, **2022**, 10, 31263-31272	3.5
3	Novel Dual Liner Process for Side-Shielded Forksheet Device With Superior Design Margin. *IEEE Transactions on Electron Devices*, **2022**, 1-4	2.9
2	Damage-induced ferroelectricity in HfOx-based thin film. *IEEE Electron Device Letters*, **2022**, 1-1	4.4
1	Analog synaptic devices applied to spiking neural networks for reinforcement learning applications. *Semiconductor Science and Technology*, **2022**, 37, 075002	1.8