Byung-Gook Park

List of Publications by Year
in descending order

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517 papers	7,665 citations	117453 34 h-index	88477 70 g-index
519 all docs	519 docs citations	519 times ranked	4297 citing authors

#	Article	IF	Citations
1	Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec. IEEE Electron Device Letters, 2007, 28, 743-745.	2.2	1,537
2	Demonstration of L-Shaped Tunnel Field-Effect Transistors. IEEE Transactions on Electron Devices, 2016, 63, 1774-1778.	1.6	250
3	Analog Synaptic Behavior of a Silicon Nitride Memristor. ACS Applied Materials & Interfaces, 2017, 9, 40420-40427.	4.0	198
4	A three-dimensional simulation of quantum transport in silicon nanowire transistor in the presence of electron-phonon interactions. Journal of Applied Physics, 2006, 99, 123719.	1.1	176
5	A new charge pump without degradation in threshold voltage due to body effect [memory applications]. IEEE Journal of Solid-State Circuits, 2000, 35, 1227-1230.	3.5	173
6	Design optimization of gate-all-around (GAA) MOSFETs. IEEE Nanotechnology Magazine, 2006, 5, 186-191.	1.1	98
7	Neuronal dynamics in HfO_x/AlO_y-based homeothermic synaptic memristors with low-power and homogeneous resistive switching. Nanoscale, 2019, 11, 237-245.	2.8	93
8	Hysteresis mechanism and reduction method in the bottom-contact pentacene thin-film transistors with cross-linked poly(vinyl alcohol) gate insulator. Applied Physics Letters, 2006, 88, 252102.	1.5	86
9	Resistive switching characteristics of Si3N4-based resistive-switching random-access memory cell with tunnel barrier for high density integration and low-power applications. Applied Physics Letters, 2015, 106, .	1.5	77
10	Scaling Effect on Silicon Nitride Memristor with Highly Doped Si Substrate. Small, 2018, 14, e1704062.	5.2	74
11	100-nm n-/p-channel I-MOS using a novel self-aligned structure. IEEE Electron Device Letters, 2005, 26, 261-263.	2.2	71
12	Double-Gate TFET With Vertical Channel Sandwiched by Lightly Doped Si. IEEE Transactions on Electron Devices, 2019, 66, 1656-1661.	1.6	71
13	Nonlinear and multilevel resistive switching memory in Ni/Si3N4/Al2O3/TiN structures. Applied Physics Letters, 2016, 108, .	1.5	67
14	Silicon-Based Floating-Body Synaptic Transistor With Frequency-Dependent Short- and Long-Term Memories. IEEE Electron Device Letters, 2016, 37, 249-252.	2.2	67
15	Spiking Neural Network Using Synaptic Transistors and Neuron Circuits for Pattern Recognition With Noisy Images. IEEE Electron Device Letters, 2018, 39, 630-633.	2.2	64
16	Three-Dimensional nand Flash Architecture Design Based on Single-Crystalline STacked ARray. IEEE Transactions on Electron Devices, 2012, 59, 35-45.	1.6	61
17	Silicon synaptic transistor for hardware-based spiking neural network and neuromorphic system. Nanotechnology, 2017, 28, 405202.	1.3	60
18	Hysteresis mechanism in pentacene thin-film transistors with poly(4-vinyl phenol) gate insulator. Applied Physics Letters, 2006, 89, 262120.	1.5	57

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19	Accurate analysis of conduction and resistive-switching mechanisms in double-layered resistive-switching memory devices. Applied Physics Letters, 2012, 101, .	1.5	57
20	Charge decay characteristics of silicon-oxide-nitride-oxide-silicon structure at elevated temperatures and extraction of the nitride trap density distribution. Applied Physics Letters, 2004, 85, 660-662.	1.5	53
21	Synaptic Characteristics of Amorphous Boron Nitride-Based Memristors on a Highly Doped Silicon Substrate for Neuromorphic Engineering. ACS Applied Materials & Interfaces, 2020, 12, 33908-33916.	4.0	52
22	Comprehensive analysis of retention characteristics in 3-D NAND flash memory cells with tube-type poly-Si channel structure. , 2015, , .		51
23	Understanding rectifying and nonlinear bipolar resistive switching characteristics in Ni/SiN_x/p-Si memory devices. RSC Advances, 2017, 7, 17882-17888.	1.7	49
24	High-Density and Near-Linear Synaptic Device Based on a Reconfigurable Gated Schottky Diode. IEEE Electron Device Letters, 2017, 38, 1153-1156.	2.2	49
25	Adaptive learning rule for hardware-based deep neural networks using electronic synapse devices. Neural Computing and Applications, 2019, 31, 8101-8116.	3.2	47
26	Low frequency noise characteristics of resistor- and Si MOSFET-type gas sensors fabricated on the same Si wafer with In2O3 sensing layer. Sensors and Actuators B: Chemical, 2020, 318, 128087.	4.0	45
27	Compact Design of Low Power Standard Ternary Inverter Based on OFF-State Current Mechanism Using Nano-CMOS Technology. IEEE Transactions on Electron Devices, 2015, 62, 2396-2403.	1.6	44
28	Filamentary and interface switching of CMOS-compatible Ta2O5 memristor for non-volatile memory and synaptic devices. Applied Surface Science, 2020, 529, 147167.	3.1	44
29	70-nm impact-ionization metal-oxide-semiconductor (I-MOS) devices integrated with tunneling field-effect transistors (TFETs). , 0, , .		43
30	Silicon single-electron transistors with sidewall depletion gates and their application to dynamic single-electron transistor logic. IEEE Transactions on Electron Devices, 2002, 49, 627-635.	1.6	41
31	Zinc Tin Oxide Synaptic Device for Neuromorphic Engineering. IEEE Access, 2020, 8, 130678-130686.	2.6	41
32	A New Capacitorless 1T DRAM Cell: Surrounding Gate MOSFET With Vertical Channel (SGVC Cell). IEEE Nanotechnology Magazine, 2007, 6, 352-357.	1.1	39
33	System-Level Simulation of Hardware Spiking Neural Network Based on Synaptic Transistors and I&F Neuron Circuits. IEEE Electron Device Letters, 2018, 39, 1441-1444.	2.2	37
34	3-D Stacked Synapse Array Based on Charge-Trap Flash Memory for Implementation of Deep Neural Networks. IEEE Transactions on Electron Devices, 2019, 66, 420-427.	1.6	37
35	Silicon-compatible compound semiconductor tunneling field-effect transistor for high performance and low standby power operation. Applied Physics Letters, 2011, 99, .	1.5	36
36	Light Effect on Negative Bias-Induced Instability of HfInZnO Amorphous Oxide Thin-Film Transistor. IEEE Transactions on Electron Devices, 2011, 58, 1127-1133.	1.6	36

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37	Comparison of the characteristics of semiconductor gas sensors with different transducers fabricated on the same substrate. Sensors and Actuators B: Chemical, 2021, 335, 129661.	4.0	36
38	Low hysteresis pentacene thin-film transistors using SiO2/cross-linked poly(vinyl alcohol) gate dielectric. Applied Physics Letters, 2006, 89, 263507.	1.5	35
39	A Simple Figure of Merit of RF MOSFET for Low-Noise Amplifier Design. IEEE Electron Device Letters, 2008, 29, 1380-1382.	2.2	35
40	Reset-voltage-dependent precise tuning operation of TiOx/Al2O3 memristive crossbar array. Applied Physics Letters, 2020, 117, .	1.5	35
41	Fully Si compatible SiN resistive switching memory with large self-rectification ratio. AIP Advances, 2016, 6, .	0.6	33
42	Integrate-and-fire neuron circuit using positive feedback field effect transistor for low power operation. Journal of Applied Physics, 2018, 124, .	1.1	33
43	Fabrication and program/erase characteristics of 30-nm SONOS nonvolatile memory devices. IEEE Nanotechnology Magazine, 2003, 2, 258-264.	1.1	32
44	3-D Floating-Gate Synapse Array With Spike-Time-Dependent Plasticity. IEEE Transactions on Electron Devices, 2018, 65, 101-107.	1.6	32
45	High-Density and Highly-Reliable Binary Neural Networks Using NAND Flash Memory Cells as Synaptic Devices. , 2019, , .		32
46	On-Chip Training Spiking Neural Networks Using Approximated Backpropagation With Analog Synaptic Devices. Frontiers in Neuroscience, 2020, 14, 423.	1.4	32
47	AND Flash Array Based on Charge Trap Flash for Implementation of Convolutional Neural Networks. IEEE Electron Device Letters, 2020, 41, 1653-1656.	2.2	32
48	Threshold Voltage Fluctuation by Random Telegraph Noise in Floating Gate nand Flash Memory String. IEEE Transactions on Electron Devices, 2011, 58, 67-73.	1.6	31
49	Compact Neuromorphic System With Four-Terminal Si-Based Synaptic Devices for Spiking Neural Networks. IEEE Transactions on Electron Devices, 2017, 64, 2438-2444.	1.6	31
50	Adaptive Weight Quantization Method for Nonlinear Synaptic Devices. IEEE Transactions on Electron Devices, 2019, 66, 395-401.	1.6	31
51	Proposition of deposition and bias conditions for optimal signal-to-noise-ratio in resistor- and FET-type gas sensors. Nanoscale, 2020, 12, 19768-19775.	2.8	31
52	Investigation of Electrical Characteristic Behavior Induced by Channel-Release Process in Stacked Nanosheet Gate-All-Around MOSFETs. IEEE Transactions on Electron Devices, 2020, 67, 2648-2652.	1.6	31
53	Improved resistive switching characteristics in Ni/SiNx/p++-Si devices by tuning x. Applied Physics Letters, 2017, 111, .	1.5	30
54	A practical SPICE model based on the physics and characteristics of realistic single-electron transistors. IEEE Nanotechnology Magazine, 2002, 1, 226-232.	1.1	29

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55	Three-Dimensional NAND Flash Memory Based on Single-Crystalline Channel Stacked Array. IEEE Electron Device Letters, 2013, 34, 990-992.	2.2	29
56	Operation Scheme of Multi-Layer Neural Networks Using NAND Flash Memory as High-Density Synaptic Devices. IEEE Journal of the Electron Devices Society, 2019, 7, 1085-1093.	1.2	29
57	A New Programming Method to Alleviate the Program Speed Variation in Three-Dimensional Stacked Array NAND Flash Memory. Journal of Semiconductor Technology and Science, 2014, 14, 566-571.	0.1	29
58	Enhancement of Memory Performance Using Doubly Stacked Si-Nanocrystal Floating Gates Prepared by Ion Beam Sputtering in UHV. IEEE Transactions on Electron Devices, 2007, 54, 359-362.	1.6	28
59	Modeling and Parameter Extraction for the Series Resistance in Thin-Film Transistors. IEEE Transactions on Electron Devices, 2009, 56, 431-440.	1.6	28
60	Effects of conducting defects on resistive switching characteristics of SiNx-based resistive random-access memory with MIS structure. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2015, 33, .	0.6	28
61	Multilevel switching memristor by compliance current adjustment for off-chip training of neuromorphic system. Chaos, Solitons and Fractals, 2021, 153, 111587.	2.5	28
62	Effects of High-Pressure Annealing on the Low-Frequency Noise Characteristics in Ferroelectric FET. IEEE Electron Device Letters, 2022, 43, 13-16.	2.2	28
63	Implementation of Short-Term Plasticity and Long-Term Potentiation in a Synapse Using Si-Based Type of Charge-Trap Memory. IEEE Transactions on Electron Devices, 2015, 62, 569-573.	1.6	27
64	Nano-cone resistive memory for ultralow power operation. Nanotechnology, 2017, 28, 125207.	1.3	27
65	Ultralow power switching in a silicon-rich SiN_y/SiN_x double-layer resistive memory device. Physical Chemistry Chemical Physics, 2017, 19, 18988-18995.	1.3	27
66	Self-gating effects in carbon nanotube network based liquid gate field effect transistors. Applied Physics Letters, 2008, 93, .	1.5	26
67	A study on the carrier injection mechanism of the bottom-contact pentacene thin film transistor. Applied Physics Letters, 2010, 96, .	1.5	26
68	Complementary Silicon Nanowire Hydrogen Ion Sensor With High Sensitivity and Voltage Output. IEEE Electron Device Letters, 2012, 33, 1768-1770.	2.2	26
69	Gradual bipolar resistive switching in Ni/Si3N4/n+-Si resistive-switching memory device for high-density integration and low-power applications. Solid-State Electronics, 2015, 114, 94-97.	0.8	26
70	Reconfigurable Field-Effect Transistor as a Synaptic Device for XNOR Binary Neural Network. IEEE Electron Device Letters, 2019, 40, 624-627.	2.2	26
71	Improved signal-to-noise-ratio of FET-type gas sensors using body bias control and embedded micro-heater. Sensors and Actuators B: Chemical, 2021, 329, 129166.	4.0	26
72	Admittance Measurements on OFET Channel and Its Modeling With <formula formulatype="inline"><tex>R</tex></formula>–<formula formulatype="inline"><tex>C</tex></formula> Network. IEEE Electron Device Letters, 2007, 28, 204-206.	2.2	25

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73	Simulation of the effect of parasitic channel height on characteristics of stacked gate-all-around nanosheet FET. Solid-State Electronics, 2020, 164, 107686.	0.8	25
74	Ferroelectric-Gate Field-Effect Transistor Memory With Recessed Channel. IEEE Electron Device Letters, 2020, 41, 1201-1204.	2.2	25
75	Improvement in Self-Heating Characteristic by Incorporating Hetero-Gate-Dielectric in Gate-All-Around MOSFETs. IEEE Journal of the Electron Devices Society, 2021, 9, 36-41.	1.2	25
76	3-bit multilevel operation with accurate programming scheme in TiO _x /Al₂O₃ memristor crossbar array for quantized neuromorphic system. Nanotechnology, 2021, 32, 295201.	1.3	25
77	4â€bit Multilevel Operation in Overshoot Suppressed Al₂O₃/TiO_x Resistive Randomâ€Access Memory Crossbar Array. Advanced Intelligent Systems, 2022, 4, .	3.3	25
78	Single-Crystalline Si STacked ARray (STAR) NAND Flash Memory. IEEE Transactions on Electron Devices, 2011, 58, 1006-1014.	1.6	24
79	Effects of Localized Body Doping on Switching Characteristics of Tunnel FET Inverters With Vertical Structures. IEEE Transactions on Electron Devices, 2017, 64, 1799-1805.	1.6	24
80	Current suppressed self-compliance characteristics of oxygen rich TiOy inserted Al2O3/TiOx based RRAM. Applied Physics Letters, 2020, 117, .	1.5	24
81	The Compact Modeling of Channel Potential in Sub-30-nm NAND Flash Cell String. IEEE Electron Device Letters, 2012, 33, 321-323.	2.2	23
82	Gradual switching and self-rectifying characteristics of Cu/Î±-IGZO/p+-Si RRAM for synaptic device application. Solid-State Electronics, 2018, 150, 60-65.	0.8	23
83	Design and Optimization of Triple-k Spacer Structure in Two-Stack Nanosheet FET From OFF-State Leakage Perspective. IEEE Transactions on Electron Devices, 2020, 67, 1317-1322.	1.6	23
84	Electrical characteristics of FinFET with vertically nonuniform source/drain doping profile. IEEE Nanotechnology Magazine, 2002, 1, 233-237.	1.1	22
85	Twin SONOS Memory With 30-nm Storage Nodes Under a Merged Gate Fabricated With Inverted Sidewall and Damascene Process. IEEE Electron Device Letters, 2004, 25, 317-319.	2.2	22
86	Si-Based FET-Type Synaptic Device With Short-Term and Long-Term Plasticity Using High-<inline-formula> <tex-math notation="LaTeX">$kappa$ </tex-math> </inline-formula> Gate-Stack. IEEE Transactions on Electron Devices, 2019, 66, 917-923.	1.6	22
87	A Proposal on an Optimized Device Structure With Experimental Studies on Recent Devices for the DRAM Cell Transistor. IEEE Transactions on Electron Devices, 2007, 54, 3325-3335.	1.6	21
88	An Accurate Compact Model Considering Direct-Channel Interference of Adjacent Cells in Sub-30-nm nand Flash Technologies. IEEE Electron Device Letters, 2012, 33, 1114-1116.	2.2	21
89	Vertical type double gate tunnelling FETs with thin tunnel barrier. Electronics Letters, 2015, 51, 718-720.	0.5	21
90	Implementation of Boolean Logic Functions in Charge Trap Flash for In-Memory Computing. IEEE Electron Device Letters, 2019, 40, 1358-1361.	2.2	21

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91	Uniformity Improvement of SiN _x -Based Resistive Switching Memory by Suppressed Internal Overshoot Current. IEEE Nanotechnology Magazine, 2018, 17, 824-828.	1.1	20
92	Realization of Biomimetic Synaptic Functions in a One-Cell Organic Resistive Switching Device Using the Diffusive Parameter of Conductive Filaments. ACS Applied Materials & Interfaces, 2020, 12, 51719-51728.	4.0	20
93	Sensitivity Analysis Based on Neural Network for Optimizing Device Characteristics. IEEE Electron Device Letters, 2020, 41, 1548-1551.	2.2	20
94	Investigation of Sidewall High-k Interfacial Layer Effect in Gate-All-Around Structure. IEEE Transactions on Electron Devices, 2020, 67, 1859-1863.	1.6	20
95	Efficient fusion of spiking neural networks and FET-type gas sensors for a fast and reliable artificial olfactory system. Sensors and Actuators B: Chemical, 2021, 345, 130419.	4.0	20
96	Comprehensive and accurate analysis of the working principle in ferroelectric tunnel junctions using low-frequency noise spectroscopy. Nanoscale, 2022, 14, 2177-2185.	2.8	20
97	Ultrathin gate oxide grown on nitrogen-implanted silicon for deep submicron CMOS transistors. IEEE Transactions on Electron Devices, 2001, 48, 2310-2316.	1.6	19
98	Threshold-Voltage Modeling of Body-Tied FinFETs (Bulk FinFETs). IEEE Transactions on Electron Devices, 2007, 54, 537-545.	1.6	19
99	Demonstration of Fin-Tunnel Field-Effect Transistor with Elevated Drain. Micromachines, 2019, 10, 30.	1.4	19
100	Fabrication and Characterization of TiO_x Memristor for Synaptic Device Application. IEEE Nanotechnology Magazine, 2020, 19, 475-480.	1.1	19
101	Memristive and Synaptic Characteristics of Nitride-Based Heterostructures on Si Substrate. Nanomaterials, 2020, 10, 994.	1.9	19
102	Capacitor-Based Synaptic Devices for Hardware Spiking Neural Networks. IEEE Electron Device Letters, 2022, 43, 549-552.	2.2	19
103	Neuromorphic Technology Based on Charge Storage Memory Devices. , 2018, , .		18
104	A Low-Energy High-Density Capacitor-Less I&F Neuron Circuit Using Feedback FET Co-Integrated With CMOS. IEEE Journal of the Electron Devices Society, 2019, 7, 1080-1084.	1.2	18
105	Effect of charge storage engineering on the NO₂ gas sensing properties of a WO₃ FET-type gas sensor with a horizontal floating-gate. Nanoscale, 2021, 13, 9009-9017.	2.8	18
106	Effect of Program Error in Memristive Neural Network With Weight Quantization. IEEE Transactions on Electron Devices, 2022, 69, 3151-3157.	1.6	18
107	The effects of deuterium annealing on the reduction of dark currents in the CMOS APS. IEEE Transactions on Electron Devices, 2004, 51, 1346-1349.	1.6	17
108	Design and Fabrication of Asymmetric MOSFETs Using a Novel Self-Aligned Structure. IEEE Transactions on Electron Devices, 2007, 54, 2969-2974.	1.6	17

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109	Independent Double-Gate Fin SONOS Flash Memory Fabricated With Sidewall Spacer Patterning. IEEE Transactions on Electron Devices, 2009, 56, 1721-1728.	1.6	17
110	Suppression of Read Disturb Fail Caused by Boosting Hot Carrier Injection Effect for 3-D Stack NAND Flash Memories. IEEE Electron Device Letters, 2014, 35, 42-44.	2.2	17
111	Twin-bit silicon-oxide-nitride-oxide-silicon (sSONOS) memory by inverted sidewall patterning (TSM-ISp). IEEE Nanotechnology Magazine, 2003, 2, 246-252.	1.1	16
112	Power- and Low-Resistance-State-Dependent, Bipolar Reset-Switching Transitions in SiN-Based Resistive Random-Access Memory. Nanoscale Research Letters, 2016, 11, 360.	3.1	16
113	Vertically Stacked Gate-All-Around Structured Tunneling-Based Ternary-CMOS. IEEE Transactions on Electron Devices, 2020, 67, 3889-3893.	1.6	16
114	3-D AND-Type Flash Memory Architecture With High-Î¹ Gate Dielectric for High-Density Synaptic Devices. IEEE Transactions on Electron Devices, 2021, 68, 3801-3806.	1.6	16
115	Effect of traps on transient bit-line current behavior in word-line stacked nand flash memory with poly-Si body. , 2014, , .		15
116	Self-Compliant Bipolar Resistive Switching in SiN-Based Resistive Switching Memory. Materials, 2017, 10, 459.	1.3	15
117	Vertical-Structured Electron-Hole Bilayer Tunnel Field-Effect Transistor for Extremely Low-Power Operation With High Scalability. IEEE Transactions on Electron Devices, 2018, 65, 2010-2015.	1.6	15
118	Highly Reliable Inference System of Neural Networks Using Gated Schottky Diodes. IEEE Journal of the Electron Devices Society, 2019, 7, 522-528.	1.2	15
119	Impact of the Sub-Resting Membrane Potential on Accurate Inference in Spiking Neural Networks. Scientific Reports, 2020, 10, 3515.	1.6	15
120	Low-power and reliable gas sensing system based on recurrent neural networks. Sensors and Actuators B: Chemical, 2021, 340, 129258.	4.0	15
121	Ferroelectricity of pure HfOx in metal-ferroelectric-insulator-semiconductor stacks and its memory application. Applied Surface Science, 2022, 573, 151566.	3.1	15
122	Fully integrated FET-type gas sensor with optimized signal-to-noise ratio for H2S gas detection. Sensors and Actuators B: Chemical, 2022, 367, 132052.	4.0	15
123	80nm self-aligned complementary I-MOS using double sidewall spacer and elevated drain structure and its applicability to amplifiers with high linearity. , 0, , .		14
124	SET/CMOS Hybrid Process and Multiband Filtering Circuits. IEEE Transactions on Electron Devices, 2005, 52, 1845-1850.	1.6	14
125	Investigation on the characteristics of stress-induced hump in amorphous oxide thin film transistors. Applied Physics Letters, 2011, 99, 043502.	1.5	14
126	Analysis on Program Disturbance in Channel-Stacked NAND Flash Memory With Layer Selection by Multilevel Operation. IEEE Transactions on Electron Devices, 2016, 63, 1041-1046.	1.6	14

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127	Dual Functions of V/SiOx/AlOy/p++Si Device as Selector and Memory. Nanoscale Research Letters, 2018, 13, 252.	3.1	14
128	Space Program Scheme for 3-D NAND Flash Memory Specialized for the TLC Design. , 2018, , .		14
129	SiO2 layer effect on atomic layer deposition Al2O3-based resistive switching memory. Applied Physics Letters, 2019, 114, 182102.	1.5	14
130	A Band-Engineered One-Transistor DRAM With Improved Data Retention and Power Efficiency. IEEE Electron Device Letters, 2019, 40, 562-565.	2.2	14
131	Demonstration of Tunneling Field-Effect Transistor Ternary Inverter. IEEE Transactions on Electron Devices, 2020, 67, 4541-4544.	1.6	14
132	Optimization of post-deposition annealing temperature for improved signal-to-noise ratio in In₂O₃ gas sensor. Semiconductor Science and Technology, 2021, 36, 075007.	1.0	14
133	Electrical and Thermal Performances of Omega-Shaped-Gate Nanowire Field Effect Transistors for Low Power Operation. Journal of Nanoscience and Nanotechnology, 2020, 20, 4092-4096.	0.9	14
134	Effects of Channel Length Scaling on the Signal-to-Noise Ratio in FET-Type Gas Sensor With Horizontal Floating-Gate. IEEE Electron Device Letters, 2022, 43, 442-445.	2.2	14
135	Silicon-Based Field-Induced Band-to-Band Tunneling Effect Transistor. IEEE Electron Device Letters, 2004, 25, 439-441.	2.2	13
136	Investigation of Gate Etch Damage at Metal/High-k Gate Dielectric Stack Through Random Telegraph Noise in Gate Edge Direct Tunneling Current. IEEE Electron Device Letters, 2011, 32, 569-571.	2.2	13
137	SiNW-CMOS Hybrid Common-Source Amplifier as a Voltage-Readout Hydrogen Ion Sensor. IEEE Electron Device Letters, 2013, 34, 135-137.	2.2	13
138	Characterization of a Capacitorless DRAM Cell for Cryogenic Memory Applications. IEEE Electron Device Letters, 2019, 40, 1614-1617.	2.2	13
139	Surface Ge-rich p-type SiGe channel tunnel field-effect transistor fabricated by local condensation technique. Solid-State Electronics, 2020, 164, 107701.	0.8	13
140	Effects of Process-Induced Defects on Polarization Switching in Ferroelectric Tunneling Junction Memory. IEEE Electron Device Letters, 2021, 42, 323-326.	2.2	13
141	A More Hardware-Oriented Spiking Neural Network Based on Leading Memory Technology and Its Application With Reinforcement Learning. IEEE Transactions on Electron Devices, 2021, 68, 4411-4417.	1.6	13
142	Design and optimization of two-bit double-gate nonvolatile memory cell for highly reliable operation. IEEE Nanotechnology Magazine, 2006, 5, 180-185.	1.1	12
143	Design and Characterization of Semi-Floating-Gate Synaptic Transistor. Micromachines, 2019, 10, 32.	1.4	12
144	Low-Power and High-Density Neuron Device for Simultaneous Processing of Excitatory and Inhibitory Signals in Neuromorphic Systems. IEEE Access, 2020, 8, 202639-202647.	2.6	12

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145	Analysis on Reverse Drain-Induced Barrier Lowering and Negative Differential Resistance of Ferroelectric-Gate Field-Effect Transistor Memory. IEEE Electron Device Letters, 2020, 41, 1197-1200.	2.2	12
146	Hardware-based spiking neural network architecture using simplified backpropagation algorithm and homeostasis functionality. Neurocomputing, 2021, 428, 153-165.	3.5	12
147	Multiplexed Silicon Nanowire Tunnel FET-Based Biosensors With Optimized Multi-Sensing Currents. IEEE Sensors Journal, 2021, 21, 8839-8846.	2.4	12
148	Optimization of channel structure and bias condition for signal-to-noise ratio improvement in Si-based FET-type gas sensor with horizontal floating-gate. Sensors and Actuators B: Chemical, 2022, 357, 131398.	4.0	12
149	Investigation of Low-Frequency Noise Characteristics of Ferroelectric Tunnel Junction: From Conduction Mechanism and Scaling Perspectives. IEEE Electron Device Letters, 2022, 43, 958-961.	2.2	12
150	Negative-differential transconductance characteristics at room temperature in 30-nm square-channel SOI nMOSFETs with a degenerately doped body. IEEE Electron Device Letters, 2002, 23, 612-614.	2.2	11
151	Performance improvement of scaled-down top-contact OTFTs by two-step-deposition of pentacene. IEEE Electron Device Letters, 2005, 26, 903-905.	2.2	11
152	Quantum simulation of noise in silicon nanowire transistors with electron-phonon interactions. Journal of Applied Physics, 2009, 105, .	1.1	11
153	Analysis of hysteresis characteristics of silicon nanowire biosensors in aqueous environment. Applied Physics Letters, 2011, 99, 252103.	1.5	11
154	Pulse area dependent gradual resistance switching characteristics of CMOS compatible SiN x -based resistive memory. Solid-State Electronics, 2017, 132, 109-114.	0.8	11
155	Efficient precise weight tuning protocol considering variation of the synaptic devices and target accuracy. Neurocomputing, 2020, 378, 189-196.	3.5	11
156	Negative Capacitance Effect on MOS Structure: Influence of Electric Field Variation. IEEE Nanotechnology Magazine, 2020, 19, 168-171.	1.1	11
157	Analog Complementary Metalâ€“Oxideâ€“Semiconductor Integrate-and-Fire Neuron Circuit for Overflow Retaining in Hardware Spiking Neural Networks. Journal of Nanoscience and Nanotechnology, 2020, 20, 3117-3122.	0.9	11
158	Impacts of Program/Erase Cycling on the Low-Frequency Noise Characteristics of Reconfigurable Gated Schottky Diodes. IEEE Electron Device Letters, 2021, 42, 863-866.	2.2	11
159	Interlayer engineering for enhanced ferroelectric tunnel junction operations in HfO _x -based metal-ferroelectric-insulator-semiconductor stack. Nanotechnology, 2021, 32, 495203.	1.3	11
160	Core-Shell Dual-Gate Nanowire Memory as a Synaptic Device for Neuromorphic Application. IEEE Journal of the Electron Devices Society, 2021, 9, 1282-1289.	1.2	11
161	Simulation of Gate-All-Around Tunnel Field-Effect Transistor with an n-Doped Layer. IEICE Transactions on Electronics, 2010, E93-C, 540-545.	0.3	11
162	Investigation of Device Performance for Fin Angle Optimization in FinFET and Gate-All-Around FETs for 3 nm-Node and Beyond. IEEE Transactions on Electron Devices, 2022, 69, 2088-2093.	1.6	11

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163	Synergistic improvement of sensing performance in ferroelectric transistor gas sensors using remnant polarization. Materials Horizons, 2022, 9, 1623-1630.	6.4	11
164	Optimization of the structural complexity of artificial neural network for hardware-driven neuromorphic computing application. Applied Intelligence, 2023, 53, 6288-6306.	3.3	11
165	A Vertical 4-Bit SONOS Flash Memory and a Unique 3-D Vertical nor Array Structure. IEEE Nanotechnology Magazine, 2010, 9, 70-77.	1.1	10
166	A novel SiNW/CMOS hybrid biosensor for high sensitivity/low noise. , 2013, , .		10
167	High-Density Reconfigurable Devices With Programmable Bottom-Gate Array. IEEE Electron Device Letters, 2017, 38, 564-567.	2.2	10
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