Andy Ye

List of Publications by Year
in descending order

27	91	1937685 4	1588992 8
papers	citations	h-index	g-index

27	27	27	53
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	The effect of gate voltage boosting on the power efficiency of multi-context FPGAs. The Integration VLSI Journal, 2022, 86, 30-43.	2.1	0
2	Measuring the effect of track count and wire segment length on the layout area of switch blocks for tile-based FPGAs. Microprocessors and Microsystems, 2022, 92, 104563.	2.8	0
3	Static power model for CMOS and FPGA circuits. IET Computers and Digital Techniques, 2021, 15, 263-278.	1.2	1
4	Designing efficient FPGA tiles for power-constrained ultra-low-power applications. The Integration VLSI Journal, 2021, 78, 124-134.	2.1	3
5	Measuring the Accuracy of Layout Area Estimation Models of Tile-Based FPGAs in FinFET Technology. , 2020, , .		4
6	An Evaluation on the Accuracy of the Minimum-Width Transistor Area Models in Ranking the Layout Area of FPGA Architectures. ACM Transactions on Reconfigurable Technology and Systems, 2018, 11, 1-23.	2.5	12
7	An Empirical Analysis of the Fidelity of VPR Area Models. , 2016, , .		1
8	An evaluation on the accuracy of the minimum width transistor area models in ranking the layout area of FPGA architectures. , 2016, , .		7
9	Adaptive Decision Feedback Equalizer with Hexagon EOM and Jitter Detection. Circuits, Systems, and Signal Processing, 2016, 35, 2487-2501.	2.0	1
10	Minimum jitterâ€based adaptive decision feedback equaliser for gigaâ€bitâ€perâ€second serial links. Journal of Engineering, 2015, 2015, 25-30.	1.1	0
11	Minimum jitter adaptive decision feedback equalizer for 4PAM serial links. , 2015, , .		1
12	Measuring the Accuracy of Minimum Width Transistor Area in Estimating FPGA Layout Area. , 2015, , .		6
13	A new adaptive Decision Feedback Equalizer using hexagon eye-opening monitor for multi Gbps data links. , 2014, , .		0
14	Design techniques for decision feedback equalisation of multiâ€gigaâ€bitâ€perâ€second serial data links: a stateâ€ofâ€theâ€art review. IET Circuits, Devices and Systems, 2014, 8, 118-130.	1.4	21
15	New 2-D Eye-Opening Monitor for Gb/s Serial Links. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1209-1218.	3.1	11
16	An improved RC model for VLSI interconnects with applications to buffer insertion. Analog Integrated Circuits and Signal Processing, 2014, 79, 105-113.	1.4	2
17	A new simple RC modeling for on-chip interconnects with its applications to buffer insertion. , 2013, , .		0
18	A power-efficient 2-dimensional on-chip eye-opening monitor for Gbps serial links. Analog Integrated Circuits and Signal Processing, 2013, 76, 117-128.	1.4	1

#	Article	IF	Citations
19	A new CDMA transmitter for high-speed serial links. , 2013, , .		0
20	Two-dimensional eye-opening monitor for serial links. , 2013, , .		2
21	A new power-efficient CDMA-based transmitter for high-speed serial links. Analog Integrated Circuits and Signal Processing, 2012, 71, 343-348.	1.4	1
22	Hardware-software analysis of pole model features. , 2011, , .		0
23	The effect of multi-bit based connections on the area efficiency of FPGAs utilizing unidirectional routing resources. , 2010, , .		2
24	Using the Minimum Set of Input Combinations to Minimize the Area of Local Routing Networks in Logic Clusters Containing Logically Equivalent I/Os in FPGAs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 95-107.	3.1	7
25	A scalability study of fractional motion estimation for H.264 encoding. , 2010, , .		1
26	A scalable computing and memory architecture for variable block size motion estimation on Field-Programmable Gate Arrays. , 2008, , .		6
27	The effect of sparse switch patterns on the area efficiency of multi-bit routing resources in field-programmable gate arrays. , 2008, , .		1