

Andy Ye

List of Publications by Year in descending order

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Version: 2024-02-01

27
papers

91
citations

1937685
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1588992
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g-index

27
all docs

27
docs citations

27
times ranked

53
citing authors

#	ARTICLE	IF	CITATIONS
1	Design techniques for decision feedback equalisation of multi-Gigabit-per-second serial data links: a state-of-the-art review. IET Circuits, Devices and Systems, 2014, 8, 118-130.	1.4	21
2	An Evaluation on the Accuracy of the Minimum-Width Transistor Area Models in Ranking the Layout Area of FPGA Architectures. ACM Transactions on Reconfigurable Technology and Systems, 2018, 11, 1-23.	2.5	12
3	New 2-D Eye-Opening Monitor for Gb/s Serial Links. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1209-1218.	3.1	11
4	Using the Minimum Set of Input Combinations to Minimize the Area of Local Routing Networks in Logic Clusters Containing Logically Equivalent I/Os in FPGAs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 95-107.	3.1	7
5	An evaluation on the accuracy of the minimum width transistor area models in ranking the layout area of FPGA architectures. , 2016, , .		7
6	A scalable computing and memory architecture for variable block size motion estimation on Field-Programmable Gate Arrays. , 2008, , .		6
7	Measuring the Accuracy of Minimum Width Transistor Area in Estimating FPGA Layout Area. , 2015, , .		6
8	Measuring the Accuracy of Layout Area Estimation Models of Tile-Based FPGAs in FinFET Technology. , 2020, , .		4
9	Designing efficient FPGA tiles for power-constrained ultra-low-power applications. The Integration VLSI Journal, 2021, 78, 124-134.	2.1	3
10	The effect of multi-bit based connections on the area efficiency of FPGAs utilizing unidirectional routing resources. , 2010, , .		2
11	Two-dimensional eye-opening monitor for serial links. , 2013, , .		2
12	An improved RC model for VLSI interconnects with applications to buffer insertion. Analog Integrated Circuits and Signal Processing, 2014, 79, 105-113.	1.4	2
13	The effect of sparse switch patterns on the area efficiency of multi-bit routing resources in field-programmable gate arrays. , 2008, , .		1
14	A scalability study of fractional motion estimation for H.264 encoding. , 2010, , .		1
15	A new power-efficient CDMA-based transmitter for high-speed serial links. Analog Integrated Circuits and Signal Processing, 2012, 71, 343-348.	1.4	1
16	A power-efficient 2-dimensional on-chip eye-opening monitor for Gbps serial links. Analog Integrated Circuits and Signal Processing, 2013, 76, 117-128.	1.4	1
17	Minimum jitter adaptive decision feedback equalizer for 4PAM serial links. , 2015, , .		1
18	An Empirical Analysis of the Fidelity of VPR Area Models. , 2016, , .		1

#	ARTICLE	IF	CITATIONS
19	Adaptive Decision Feedback Equalizer with Hexagon EOM and Jitter Detection. Circuits, Systems, and Signal Processing, 2016, 35, 2487-2501.	2.0	1
20	Static power model for CMOS and FPGA circuits. IET Computers and Digital Techniques, 2021, 15, 263-278.	1.2	1
21	Hardware-software analysis of pole model features. , 2011, , .		0
22	A new simple RC modeling for on-chip interconnects with its applications to buffer insertion. , 2013, , .		0
23	A new CDMA transmitter for high-speed serial links. , 2013, , .		0
24	A new adaptive Decision Feedback Equalizer using hexagon eye-opening monitor for multi Gbps data links. , 2014, , .		0
25	Minimum jitter-based adaptive decision feedback equaliser for giga-bit-per-second serial links. Journal of Engineering, 2015, 2015, 25-30.	1.1	0
26	The effect of gate voltage boosting on the power efficiency of multi-context FPGAs. The Integration VLSI Journal, 2022, 86, 30-43.	2.1	0
27	Measuring the effect of track count and wire segment length on the layout area of switch blocks for tile-based FPGAs. Microprocessors and Microsystems, 2022, 92, 104563.	2.8	0