Ajay Kumar Dadoria

List of Publications by Year
in descending order

15	73	1684188 5	1720034 7
papers	citations	h-index	g-index

16	16	16	28
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Design of Low-Power Dynamic Type Latch Comparator Using 18Ânm FinFET Technology for SAR ADC. Lecture Notes in Mechanical Engineering, 2021, , 603-609.	0.4	2
2	Design and Analysis of Low-Power Adiabatic Logic Circuits by Using CNTFET Technology. Circuits, Systems, and Signal Processing, 2019, 38, 4338-4356.	2.0	9
3	Integrating flipped drain and power gating techniques for efficient FinFET logic circuits. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2018, 31, e2344.	1.9	1
4	Performance evaluation of domino logic circuits for wide fan-in gates with FinFET. Microsystem Technologies, 2018, 24, 3341-3348.	2.0	10
5	New Leakage Reduction Techniques for FinFET Technology with Its Application. Journal of Circuits, Systems and Computers, 2018, 27, 1850112.	1.5	1
6	Nanoscale: Low Power, Noise Tolerant Wide Fan-In Domino FinFET OR Logic. Journal of Nanoelectronics and Optoelectronics, 2018, 13, 562-571.	0.5	0
7	Ultra-low power FinFET-based domino circuits. International Journal of Electronics, 2017, 104, 952-967.	1.4	18
8	Integrating sleep and pass transistor logic for leakage power reduction in FinFET circuits. Journal of Computational Electronics, 2017, 16, 867-874.	2.5	12
9	Leakage Reduction by Using FinFET Technique for Nanoscale Technology Circuits. Journal of Nanoelectronics and Optoelectronics, 2017, 12, 278-285.	0.5	5
10	A novel efficient adiabatic logic design for ultra low power. , 2016, , .		5
11	Leakage Power Reduction Technique by using FinFET Technology. , 2016, , .		2
12	Low-Power High Speed 1-bit Full Adder Circuit Design. , 2016, , .		2
13	Sleepy lector: A novel approach for leakage reduction in DSM technology. , 2016, , .		4
14	Carbon NanoTube based logic gates structure for low power consumption at nano-scaled era. , 2016, , .		2
15	A Survey on Nano-Scale Double Gate CMOS Transistor. Advanced Science Letters, 2015, 21, 2830-2832.	0.2	0