Victor R Gonzalez-Diaz

List of Publications by Year
in descending order

37 papers	290 citations	1162367 8 h-index	940134 16 g-index
37 all docs	37 docs citations	37 times ranked	354 citing authors

#	Article	IF	Citations
1	SPICE synthesis of a solar cell model with irradiance and temperature evaluation. International Journal of Circuit Theory and Applications, 2022, 50, 3071-3085.	1.3	1
2	A Cooperative ADRC-Based Approach for Angular Velocity Synchronization and Load-Sharing in Servomechanisms. Energies, 2022, 15, 5121.	1.6	1
3	On-Chip Fuzzy Logic Synthesis of a New Ischemic and Non-Ischemic Heartbeat Classifier. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 476-480.	2.2	2
4	Ischemic and non-ischemic heartbeat classifier for portable automatic detection systems. IEEE Latin America Transactions, 2021, 19, 952-960.	1.2	1
5	CMOS OTA-Based Filters for Designing Fractional-Order Chaotic Oscillators. Fractal and Fractional, 2021, 5, 122.	1.6	16
6	A Methodology for Practical Design and Optimization of Class-E DC-DC Resonant Converters. IEEE Access, 2020, 8, 205568-205589.	2.6	3
7	Two New Asymmetric Boolean Chaos Oscillators with No Dependence on Incommensurate Time-Delays and Their Circuit Implementation. Symmetry, 2020, 12, 506.	1.1	9
8	A parallel auto-adaptive topology for integrated energy harvesting system. Microelectronics Journal, 2020, 98, 104736.	1.1	5
9	A 65nm Continuous-Time Sigma-Delta Modulator With Limited OTA DC Gain Compensation. IEEE Access, 2020, 8, 36464-36475.	2.6	7
10	A Behavioral Model for Solar Cells With Transient Irradiation and Temperature Assessment. IEEE Access, 2019, 7, 90882-90890.	2.6	7
11	A simple sliding-mode control circuit for buck DC-DC converters. , 2019, , .		3
12	Leader-Following Consensus and Formation Control of VTOL-UAVs with Event-Triggered Communications. Sensors, 2019, 19, 5498.	2.1	22
13	A CMOS Frequency Doubler from the Analog Cosine Mapping Function. Circuits, Systems, and Signal Processing, 2019, 38, 1506-1519.	1.2	0
14	Pipeline A/D Converter Design for 5G OFDM Communications Systems. , 2018, , .		0
15	A Fully Integrated Fuzzy Logic Algorithm for Ischemic Heartbeat Classification. , 2018, , .		4
16	System-Level Behavioral Model of a 12-Bit 1.5-Bit Per Stage Pipelined ADC Based on VerilogÂ®=-AMS. , 2018, , .		0
17	A new CMOS comparator robust to process and temperature variations for SAR ADC converters. Analog Integrated Circuits and Signal Processing, 2017, 90, 301-308.	0.9	13
18	CMOS harmonic upconverter with power management of $$2{f nd}$$ 2 nd harmonic for wideband short-range communications. Analog Integrated Circuits and Signal Processing, 2017, 90, 383-388.	0.9	1

#	Article	IF	Citations
19	New alternatives for analog implementation of fractional-order integrators, differentiators and PID controllers based on integer-order integrators. Nonlinear Dynamics, 2017, 90, 241-256.	2.7	60
20	A Verilog-A Based Fractional Frequency Synthesizer Model for Fast and Accurate Noise Assessment. Radioengineering, 2016, 25, 89-97.	0.3	4
21	Improving linearity in MOS varactor based VCOs by means of the output quiescent bias point. The Integration VLSI Journal, 2016, 55, 274-280.	1.3	7
22	Continuos Time Î£Î" modulator with efficient gain compensated integrators. Microelectronics Journal, 2016, 56, 38-45.	1.1	2
23	Design of buck DC-DC converters from the linear quadratic regulator approach. , 2016, , .		1
24	Improving GBW product on CMOS operational transconductance amplifiers by interleaved feedforward paths. Microelectronics Journal, 2015, 46, 1053-1059.	1.1	1
25	Opamp gain compensation technique for continuousâ€time Î£Î" modulators. Electronics Letters, 2014, 50, 355-356.	0.5	7
26	Attitude Stabilization of a Quadrotor by Means of Event-Triggered Nonlinear Control. Journal of Intelligent and Robotic Systems: Theory and Applications, 2014, 73, 123-135.	2.0	42
27	Analog sigmaâ€"delta modulation with Op-Amp gain compensation for nanometer technologies. Analog Integrated Circuits and Signal Processing, 2013, 76, 297-305.	0.9	2
28	Compact implementation of a three stages feedforward operational transconductance amplifier with Miller compensation. , 2013, , .		0
29	Fractional Frequency Synthesizers With Low Order Time-Variant Digital Sigma-Delta Modulator. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 969-978.	3.5	1
30	ΣΔ Modulator with op-amp gain compensation for nanometer CMOS technologies. , 2012, , .		2
31	Use of time variant digital sigma-delta for fractional frequency synthesizers. , 2011, , .		1
32	A Pseudorandom Number Generator Based on Time-Variant Recursion of Accumulators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 580-584.	2.2	10
33	Optimized reduction of spur tones in fractional frequency synthesizers. Analog Integrated Circuits and Signal Processing, 2010, 65, 245-251.	0.9	1
34	Efficient Dithering in MASH Sigma-Delta Modulators for Fractional Frequency Synthesizers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2394-2403.	3.5	42
35	Limitations of the Phase-to-Frequency-Detector in Fractional Frequency Synthesizers. , 2009, , .		0
36	Accurate models for Frequency Synthesizers. , 2008, , .		6

#	ARTICLE	IF	CITATIONS
37	Optimal dithered digital sigma-delta modulators for fractional-N frequency synthesizers. , 2007, , .		6