Gabriel Caffarena

List of Publications by Year
in descending order

37	419	1163117 8	794594 19
papers	citations	h-index	g-index

41	41	41	708
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A fault-tolerant clustering algorithm for processing data from multiple streams. Information Sciences, 2022, 584, 649-664.	6.9	7
2	Elastic Downsampling: An Adaptive Downsampling Technique to Preserve Image Quality. Electronics (Switzerland), 2021, 10, 400.	3.1	2
3	A Low-Latency, Low-Power FPGA Implementation of ECG Signal Characterization Using Hermite Polynomials. Electronics (Switzerland), 2021, 10, 2324.	3.1	9
4	FPGA acceleration of bit-true simulations for word-length optimization. , 2021, , .		0
5	Witelo: Automated generation and timing characterization of distributed-control macroblocks for high-performance FPGA designs. The Integration VLSI Journal, 2019, 68, 1-11.	2.1	0
6	High-Performance Decoding of Variable-Length Memory Data Packets for FPGA Stream Processing. , 2019, , .		3
7	Automated Timing Characterization of High-Performance Macroblocks for Latency Insensitive FPGA Designs. , 2018, , .		1
8	Correlations between physiological parameters related with kidney function and minuteâ€byâ€minute urine output. Nephrology, 2016, 21, 1034-1040.	1.6	1
9	Quantization Noise Power Estimation for Floating-Point DSP Circuits. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 593-597.	3.0	6
10	GPU-Based Acceleration of ECG Characterization Using High-Order Hermite Polynomials. Current Bioinformatics, 2016, 11, 430-439.	1.5	1
11	Iterative reconstruction for pet scanners with continuous scintillators. , 2015, 2015, 2259-62.		0
12	A Formal Method for Optimal High-Level Casting of Heterogeneous Fixed-Point Adders and Subtractors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 52-62.	2.7	9
13	Comparing scientific performance among equals. Scientometrics, 2014, 101, 1731-1745.	3.0	12
14	Self-Reconfigurable Constant Multiplier for FPGA. ACM Transactions on Reconfigurable Technology and Systems, 2013, 6, 1-17.	2.5	6
15	Tracking the pipelining-power rule along the FPGA technical literature. , 2013, , .		10
16	Fast Fixed-Point Optimization of DSP Algorithms. International Federation for Information Processing, 2012, , 182-205.	0.4	2
17	A Discrete Model for Correlation Between Quantization Noises. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 800-804.	3.0	1
18	Quantization of VLSI digital signal processing systems. Eurasip Journal on Advances in Signal Processing, 2012, 2012, .	1.7	1

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19	SQNR Estimation of Fixed-Point DSP Algorithms. Eurasip Journal on Advances in Signal Processing, 2010, 2010, .	1.7	28
20	Architectural synthesis of DSP circuits under simultaneous error and time constraints. , 2010, , .		3
21	A clustering approach to multireference alignment of single-particle projections in electron microscopy. Journal of Structural Biology, 2010, 171, 197-206.	2.8	188
22	Fast fixed-point optimization of DSP algorithms. , 2010, , .		3
23	Architectural Synthesis of Fixed-Point DSP Datapaths Using FPGAs. International Journal of Reconfigurable Computing, 2009, 2009, 1-14.	0.2	8
24	Providing Self-learning to Students of Highly Attended Electronics Courses through the Remote Access to a Microelectronics Laboratory. , 2009, , .		0
25	Behavioural Biometrics Hardware Based on Bioinformatics Matching. Advances in Intelligent and Soft Computing, 2009, , 171-178.	0.2	0
26	Fast and accurate computation of the round-off noise of linear time-invariant systems. IET Circuits, Devices and Systems, 2008, 2, 393.	1.4	29
27	A Methodology for CFD Acceleration Through Reconfigurable Hardware. , 2008, , .		5
28	Optimized Architectural Synthesis of Fixed-Point Datapaths. , 2008, , .		1
29	Fast and accurate power estimation of FPGA DSP components based on high-level switching activity models. International Journal of Electronics, 2008, 95, 653-668.	1.4	11
30	FPGA ACCELERATION FOR DNA SEQUENCE ALIGNMENT. Journal of Circuits, Systems and Computers, 2007, 16, 245-266.	1.5	20
31	Switching Activity Models for Power Estimation in FPGA Multipliers. , 2007, , 201-213.		3
32	High-Level Synthesis of Multiple Word-Length DSP Algorithms Using Heterogeneous-Resource FPGAs. , 2006, , .		10
33	Design and Implementation of a Hardware Module for Equalisation in A 4G MIMO Receiver. , 2006, , .		2
34	Optimal combined word-length allocation and architectural synthesis of digital signal processing circuits. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2006, 53, 339-343.	2.2	21
35	Optimized Synthesis of DSP Cores Combining Logic-based and Embedded FPGA Resources. , 2006, , .		0
36	FPGA for pseudorandom generator cryptanalysis. Microprocessors and Microsystems, 2006, 30, 63-71.	2.8	8

#	Article	IF	Citations
37	A Generator of High-Speed Floating-Point Modules. , 0, , .		6