Mahdi Fazeli

List of Publications by Year
in descending order

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102	1,293	567281 15	552781 26
papers	citations	h-index	g-index

103	103	103	840
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	CyEnSe: Cyclic energy-aware scheduling for energy-harvested embedded systems. Microprocessors and Microsystems, 2022, 89, 104421.	2.8	2
2	MagCiM: A Flexible and Non-Volatile Computing-in-Memory Processor for Energy-Efficient Logic Computation. IEEE Access, 2022, 10, 35445-35459.	4.2	6
3	A multi-application approach for synthesizing custom network-on-chips. Journal of Supercomputing, 2022, 78, 15358-15380.	3.6	4
4	NOSTalgy: Near-Optimum Run-Time STT-MRAM Quality-Energy Knob Management for Approximate Computing Applications. IEEE Transactions on Computers, 2021, 70, 414-427.	3.4	6
5	Joint Effects of Aging and Process Variations on Soft Error Rate of Nano-Scale Digital Circuits. Journal of Circuits, Systems and Computers, 2021, 30, 2150012.	1.5	1
6	CONFISCA: An SIMD-Based Concurrent FI and SCA Countermeasure with Switchable Performance and Security Modes. Cryptography, 2021, 5, 13.	2.3	0
7	An energy efficient synthesis flow for application specific SoC design. The Integration VLSI Journal, 2021, 81, 331-341.	2.1	3
8	An In-Depth Vulnerability Analysis of RISC-V Micro-Architecture Against Fault Injection Attack. , 2021, , .		1
9	Efficient Scheduling of Dependent Tasks in Many-Core Real-Time System Using a Hardware Scheduler. , 2021, , .		7
10	Protecting scratchpad memory addresses against soft errors. Microelectronics Reliability, 2020, 111, 113741.	1.7	1
11	A Review on Evaluation and Configuration of Fault Injection Attack Instruments to Design Attack Resistant MCU-Based IoT Applications. Electronics (Switzerland), 2020, 9, 1153.	3.1	9
12	Joint VNF Load Balancing and Service Auto-Scaling in NFV with Multimedia Case Study. , 2020, , .		1
13	Design Space Exploration for Ultra-Low-Energy and Secure IoT MCUs. Transactions on Embedded Computing Systems, 2020, 19, 1-34.	2.9	14
14	Scanâ€based attack tolerance with minimum testability loss: a gateâ€level approach. IET Information Security, 2020, 14, 459-469.	1.7	1
15	Restricting Switching Activity Using Logic Locking to Improve Power Analysis-Based Trojan Detection. , 2019, , .		1
16	Ultra-low power and reliable magnetic based interconnects for nano-scale technologies. Microelectronics Journal, 2019, 90, 39-47.	2.0	2
17	RTHS: A Low-Cost High-Performance Real-Time Hardware Sorter, Using a Multidimensional Sorting Algorithm. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1601-1613.	3.1	22
18	An Energy-Efficient Reliable Heterogeneous Uncore Architecture for Future 3D Chip-Multiprocessors. Journal of Circuits, Systems and Computers, 2019, 28, 1950224.	1.5	2

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19	Design of ultra low power current mode logic gates using magnetic cells. AEU - International Journal of Electronics and Communications, 2018, 83, 270-279.	2.9	17
20	An Efficient Programming Skeleton for Clusters of Multi-Core Processors. International Journal of Parallel Programming, 2018, 46, 1094-1109.	1.5	2
21	Pure Magnetic Logic Circuits: A Reliability Analysis. IEEE Transactions on Magnetics, 2018, 54, 1-10.	2.1	22
22	Vulnerability modelling of cryptoâ€chips against scanâ€based attacks. IET Information Security, 2018, 12, 543-550.	1.7	2
23	Hardware Trojan Detection Using an Advised Genetic Algorithm Based Logic Testing. Journal of Electronic Testing: Theory and Applications (JETTA), 2018, 34, 461-470.	1.2	34
24	Application Specific Networks-on-Chip Synthesis: An Energy Efficient Approach. , 2018, , .		2
25	Mystic: Mystifying IP Cores Using an Always-ON FSM Obfuscation Method. , 2018, , .		7
26	mGate: A Universal Magnetologic Gate for Design of Energy Efficient Digital Circuits. IEEE Transactions on Magnetics, 2017, 53, 1-13.	2.1	7
27	ARMICA-Improved: A New Approach for Association Rule Mining. Lecture Notes in Computer Science, 2017, , 296-306.	1.3	4
28	Microâ€architectural approach to the efficient employment of STTRAM cells in a microprocessor register file. IET Computers and Digital Techniques, 2017, 11, 1-7.	1.2	2
29	Energy aware and reliable STT-RAM based cache design for 3D embedded chip-multiprocessors. , 2017, , .		5
30	Reliability and Power Optimization in 3D-Stacked Cache Using a Run-Time Reconfiguration Procedure. , 2017, , .		0
31	Single event multiple upset-tolerant SRAM cell designs for nano-scale CMOS technology. Turkish Journal of Electrical Engineering and Computer Sciences, 2017, 25, 1035-1047.	1.4	23
32	RASMAP: An efficient heuristic application mapping algorithm for network-on-chips. , 2016, , .		4
33	High output hamming-distance achievement by a greedy logic masking approach. , 2016, , .		1
34	Performance/energy aware task migration algorithm for manyâ€core chips. IET Computers and Digital Techniques, 2016, 10, 165-173.	1.2	5
35	Reliability-oriented scheduling for static-priority real-time tasks in standby-sparing systems. Microprocessors and Microsystems, 2016, 45, 208-215.	2.8	15
36	A Cache-Assisted Scratchpad Memory for Multiple-Bit-Error Correction. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3296-3309.	3.1	8

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37	Phase Change Memory lifetime enhancement via online data swapping. The Integration VLSI Journal, 2016, 54, 47-55.	2.1	3
38	Hardware enlightening: No where to hide your Hardware Trojans!. , 2016, , .		13
39	Neural network based approach for time to crash prediction to cope with software aging. Journal of Systems Engineering and Electronics, 2015, 26, 407-414.	2.2	17
40	An Efficient Data Aggregation Method for Event-Driven WSNs: A Modeling and Evaluation Approach. Wireless Personal Communications, 2015, 84, 745-764.	2.7	14
41	The More the Safe, the Less the Unsafe: An efficient method to unauthenticated packets detection in WSNs. , 2015, , .		0
42	A low power hybrid MTJ/CMOS (4-2) compressor for fast arithmetic circuits. , 2015, , .		1
43	Design of Robust SRAM Cells Against Single-Event Multiple Effects for Nanometer Technologies. IEEE Transactions on Device and Materials Reliability, 2015, 15, 429-436.	2.0	69
44	Proposing a load balancing method based on Cuckoo Optimization Algorithm for energy management in cloud computing infrastructures. , 2015, , .		35
45	ICA-MMT: A load balancing method in cloud computing environment. , 2015, , .		11
46	Soft Error-Tolerant Design of MRAM-Based Nonvolatile Latches for Sequential Logics. IEEE Transactions on Magnetics, 2015, 51, 1-14.	2.1	27
47	Single Event Multiple Upset (SEMU) Tolerant Latch Designs in Presence of Process and Temperature Variations. Journal of Circuits, Systems and Computers, 2015, 24, 1550007.	1.5	34
48	SOFT ERROR RATE ESTIMATION FOR COMBINATIONAL LOGIC IN PRESENCE OF SINGLE EVENT MULTIPLE TRANSIENTS. Journal of Circuits, Systems and Computers, 2014, 23, 1450091.	1.5	19
49	Coding Last Level STT-RAM Cache for High Endurance and Low Power. IEEE Computer Architecture Letters, 2014, 13, 73-76.	1.5	28
50	Soft error estimation and mitigation of digital circuits by characterizing input patterns of logic gates. Microelectronics Reliability, 2014, 54, 1412-1420.	1.7	6
51	Low-Cost Scan-Chain-Based Technique to Recover Multiple Errors in TMR Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1454-1468.	3.1	22
52	FTSPM: A Fault-Tolerant ScratchPad Memory. , 2013, , .		23
53	I-LEACH: An efficient routing algorithm to improve performance & to reduce energy consumption in Wireless Sensor Networks. , 2013, , .		73
54	Bee-MMT: A load balancing method for power consumption management in cloud computing. , 2013, , .		30

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55	OLDA: An Efficient On-Line Data Aggregation Method for Wireless Sensor Networks. , 2013, , .		5
56	HAFTA: Highly Available Fault-Tolerant Architecture to Protect SRAM-Based Reconfigurable Devices Against Multiple Bit Upsets. IEEE Transactions on Device and Materials Reliability, 2013, 13, 203-212.	2.0	8
57	Low cost soft error hardened latch designs for nano-scale CMOS technology in presence of process variation. Microelectronics Reliability, 2013, 53, 912-924.	1.7	49
58	A parallel clustering algorithm on the star graph and its performance. Mathematical and Computer Modelling, 2013, 58, 886-897.	2.0	0
59	Application of PCR and SYBR Green Q Rti-PCR Assays for the Identification and Quantification of Chicken Meat Under Different Cooking Conditions. Food Biotechnology, 2013, 27, 249-260.	1.5	1
60	Cylindrical Silicon Nanowire Transistor Modeling Based on Adaptive Neuro-Fuzzy Inference System (ANFIS). Journal of Electrical Engineering and Technology, 2013, 8, 1163-1168.	2.0	1
61	Adaptive hybrid position/force control for grinding applications. , 2012, , .		5
62	Value-Aware low-power register file architecture. , 2012, , .		2
63	An efficient technique to tolerate MBU faults in register file of embedded processors. , 2012, , .		8
64	An efficient fault tolerant routing algorithm for binary cube interconnection networks. , 2012, , .		1
65	Memory Mapped SPM: Protecting Instruction Scratchpad Memory in Embedded Systems against Soft Errors. , 2012, , .		7
66	Efficient algorithms to accurately compute derating factors of digital circuits. Microelectronics Reliability, 2012, 52, 1215-1226.	1.7	33
67	A Low Cost circuit level fault detection technique to Full Adder design. , 2011, , .		2
68	Software-based control flow error detection and correction using branch triplication. , 2011, , .		5
69	Low Cost Concurrent Error Detection for On-Chip Memory Based Embedded Processors. , 2011, , .		2
70	Soft error rate estimation of digital circuits in the presence of Multiple Event Transients (METs). , 2011, , .		53
71	Operand Width Aware Hardware Reuse: A low cost fault-tolerant approach to ALU design in embedded processors. Microelectronics Reliability, 2011, 51, 2374-2387.	1.7	17
72	A low-overhead and reliable switch architecture for Network-on-Chips. The Integration VLSI Journal, 2010, 43, 268-278.	2.1	8

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73	Stability analysis of a peak and deep current mode buck-boost converter. , 2010, , .		0
74	A fast and accurate multi-cycle soft error rate estimation approach to resilient embedded systems design. , 2010, , .		12
75	Robust Register Caching: An Energy-Efficient Circuit-Level Technique to Combat Soft Errors in Embedded Processors. IEEE Transactions on Device and Materials Reliability, 2010, 10, 208-221.	2.0	13
76	A Fast Analytical Approach to Multi-cycle Soft Error Rate Estimation of Sequential Circuits. , 2010, , .		8
77	A Novel SET/SEU Hardened Parallel I/O Port. , 2009, , .		1
78	Low energy single event upset/single event transient-tolerant latch for deep subMicron technologies. IET Computers and Digital Techniques, 2009, 3, 289.	1.2	110
79	An energy efficient circuit level technique to protect register file from MBUs and SETs in embedded processors. , 2009, , .		17
80	Error Detection Enhancement in PowerPC Architecture-based Embedded Processors. Journal of Electronic Testing: Theory and Applications (JETTA), 2008, 24, 21-33.	1.2	8
81	A Power Efficient Approach to Fault-Tolerant Register File Design. , 2008, , .		1
82	A Low Energy Soft Error-Tolerant Register File Architecture for Embedded Processors. , 2008, , .		10
83	A novel peak and deep current mode control for two switches buck-boost converter. IEEE Applied Power Electronics Conference and Exposition, 2008, , .	0.0	3
84	FEDC: Control Flow Error Detection and Correction for Embedded Systems without Program Interruption. , 2008, , .		12
85	A Power Efficient Masking Technique for Design of Robust Embedded Systems against SEUs and SETs. , 2008, , .		2
86	B-Jump: Roller length, sequent depth, and relative energy loss using Artificial Neural Networks. Journal of Hydraulic Research/De Recherches Hydrauliques, 2007, 45, 529-537.	1.7	2
87	A Hierarchical Routing Protocol for Energy Load Balancing in Wireless Sensor Networks. , 2007, , .		9
88	Distance-Based Segmentation: An Energy-Efficient Clustering Hierarchy for Wireless Microsensor Networks. , 2007, , .		17
89	Feedback Redundancy: A Power Efficient SEU-Tolerant Latch Design for Deep Sub-Micron Technologies. , 2007, , .		72
90	Reducing Power Consumption in NoC Design with no Effect on Performance and Reliability. , 2007, , .		1

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91	A Low-Power and SEU-Tolerant Switch Architecture for Network on Chips. , 2007, , .		31
92	Combinatorial Constructions of Multi-erasure-Correcting Codes with Independent Parity Symbols for Storage Systems. , 2007, , .		15
93	A Solution to Single Point of Failure Using Voter Replication and Disagreement Detection. , 2006, , .		5
94	Experimental Evaluation of Three Concurrent Error Detection Mechanisms. , 2006, , .		1
95	A Software-Based Error Detection Technique Using Encoded Signatures. Defect and Fault Tolerance in VLSI Systems, Proceedings of the IEEE International Symposium on, 2006, , .	0.0	17
96	Performance evaluation of a routing protocol for wireless sensor networks. , 2006, , .		7
97	A Checkpointing Technique for Rollback Error Recovery in Embedded Systems. , 2006, , .		8
98	Transient Error Detection in Embedded Systems Using Reconfigurable Components. , 2006, , .		2
99	A Fault Tolerant Approach to Object Oriented Design and Synthesis of Embedded Systems. Lecture Notes in Computer Science, 2005, , 143-153.	1.3	0
100	A Cordic-Based Processor Extension for Scalar and Vector Processing. , 0, , .		1
101	Directed Flooding: A Fault-Tolerant Routing Protocol for Wireless Sensor Networks. , 0, , .		15
102	A software-based concurrent error detection technique for power PC processor-based embedded systems. , 0, , .		15