

# Christopher Batten

## List of Publications by Citations

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.

16  
papers

226  
citations

8  
h-index

15  
g-index

21  
ext. papers

336  
ext. citations

2.3  
avg, IF

3.05  
L-index

#	Paper	IF	Citations
16	Designing Chip-Level Nanophotonic Interconnection Networks. <i>IEEE Journal on Emerging and Selected Topics in Circuits and Systems</i> , <b>2012</b> , 2, 137-153	5.2	41
15	PyMTL: A Unified Framework for Vertically Integrated Computer Architecture Research <b>2014</b> ,		36
14	The Celerity Open-Source 511-Core RISC-V Tiered Accelerator Fabric: Fast Architectures and Design Methodologies for Fast Chips. <i>IEEE Micro</i> , <b>2018</b> , 38, 30-41	1.8	34
13	Enabling Realistic Fine-Grain Voltage Scaling with Reconfigurable Power Distribution Networks <b>2014</b> ,		31
12	Accelerating Irregular Algorithms on GPGPUs Using Fine-Grain Hardware Worklists <b>2014</b> ,		25
11	Architectural Specialization for Inter-Iteration Loop Dependence Patterns <b>2014</b> ,		17
10	Asymmetry-Aware Work-Stealing Runtimes <b>2016</b> ,		10
9	A 1.4 GHz 695 Giga Risc-V Inst/s 496-Core Manycore Processor With Mesh On-Chip Network and an All-Digital Synthesized PLL in 16nm CMOS <b>2019</b> ,		8
8	PyMTL3: A Python Framework for Open-Source Hardware Modeling, Generation, Simulation, and Verification. <i>IEEE Micro</i> , <b>2020</b> , 40, 58-66	1.8	6
7	Four Monolithically Integrated Switched-Capacitor DCDC Converters With Dynamic Capacitance Sharing in 65-nm CMOS. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , <b>2018</b> , 65, 2035-2047	3.9	6
6	Evaluating Celerity: A 16-nm 695 Giga-RISC-V Instructions/s Manycore Processor With Synthesizable PLL. <i>IEEE Solid-State Circuits Letters</i> , <b>2019</b> , 2, 289-292	2	5
5	Mamba: Closing the Performance Gap in Productive Hardware Development Frameworks <b>2018</b> ,		4
4	PyOCN: A Unified Framework for Modeling, Testing, and Evaluating On-Chip Networks <b>2019</b> ,		3
3	Cross-layer workload characterization of meta-tracing JIT VMs <b>2017</b> ,		0
2	PyH2: Using PyMTL3 to Create Productive and Open-Source Hardware Testing Methodologies. <i>IEEE Design and Test</i> , <b>2021</b> , 38, 53-61	1.4	0
1	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2021</b> , 1-1	2.5	0