Aijiao Cui

List of Publications by Year
in descending order

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30 papers	334 citations	1478505 6 h-index	1720034 7 g-index
30 all docs	30 docs citations	30 times ranked	163 citing authors

#	Article	IF	Citations
1	A Robust FSM Watermarking Scheme for IP Protection of Sequential Circuit Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 678-690.	2.7	81
2	Static and Dynamic Obfuscations of Scan Data Against Scan-Based Side-Channel Attacks. IEEE Transactions on Information Forensics and Security, 2017, 12, 363-376.	6.9	55
3	Ultra-Low Overhead Dynamic Watermarking on Scan Design for Hard IP Protection. IEEE Transactions on Information Forensics and Security, 2015, 10, 2298-2313.	6.9	36
4	A New PUF Based Lock and Key Solution for Secure In-Field Testing of Cryptographic Chips. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 1095-1105.	4.6	25
5	A new countermeasure against scan-based side-channel attacks. , 2016, , .		17
6	A Guaranteed Secure Scan Design Based on Test Data Obfuscation by Cryptographic Hash. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4524-4536.	2.7	16
7	A New Active IC Metering Technique Based on Locking Scan Cells. , 2017, , .		13
8	Design of Optimal Scan Tree Based on Compact Test Patterns for Test Time Reduction. IEEE Transactions on Computers, 2015, 64, 3417-3429.	3.4	11
9	A New Pay-Per-Use Scheme for the Protection of FPGA IP. , 2019, , .		10
10	A new decompressor with ordered parallel scan design for reduction of test data and test time. , 2015, , .		7
11	Partial Scan Design Against Scan-Based Side Channel Attacks. , 2018, , .		7
12	Reliable and Anti-cloning PUFs Based on Configurable Ring Oscillators. , 2015, , .		6
13	A new watermarking scheme on scan chain ordering for hard IP protection. , 2017, , .		6
14	A Secure and Low-overhead Active IC Metering Scheme. , 2019, , .		6
15	Novel Memristor-based Nonvolatile D Latch and Flip-flop Designs. , 2021, , .		6
16	An improved scan cell ordering method using the scan cells with complementary outputs. , 2014, , .		5
17	Balancing Testability and Security by Configurable Partial Scan Design. , 2018, , .		4
18	A New Secure Scan Design with PUF-based Key for Authentication. , 2020, , .		4

#	Article	IF	Citations
19	An improved scan design for minimization of test power under routing constraint. , 2015, , .		3
20	How to Secure Scan Design Against Scan-Based Side-Channel Attacks?. , 2017, , .		3
21	SATAM: A SAT Attack Resistant Active Metering Against IC Overbuilding. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 2025-2041.	4.6	3
22	A power-efficient scan tree design by exploring the Q'-D connection. , 2013, , .		2
23	An ultra-low overhead LUT-based PUF for FPGA. , 2016, , .		2
24	A Memristor-based Scan Hold Flip-Flop. , 2019, , .		2
25	Identification of State Registers of FSM Through Full Scan by Data Analytics. , 2019, , .		2
26	A low-overhead dynamic watermarking scheme on scan design for easy authentication. , 2014, , .		1
27	A Low-Cost Fault Injection Attack Resilient FSM Design. , 2020, , .		1
28	How to Retrieve PUF Response from a Fabricated Chip Securely?. , 2020, , .		0
29	Identification of FSM State Registers by Analytics of Scan-Dump Data. IEEE Transactions on Information Forensics and Security, 2021, 16, 5138-5153.	6.9	0
30	A Memristor-based Secure Scan Design against the Scan-based Side-Channel Attacks. , 2022, , .		0