Angie Wang

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/367199/publications.pdf

Version: 2024-02-01

7 papers	133 citations	2258059 3 h-index	2550090 3 g-index
7 all docs	7 docs citations	7 times ranked	85 citing authors

#	Article	IF	Citations
1	Reusability is FIRRTL ground: Hardware construction languages, compiler frameworks, and transformations. , 2017, , .		98
2	A Mixed-Signal RISC-V Signal Analysis SoC Generator With a 16-nm FinFET Instance. IEEE Journal of Solid-State Circuits, 2019, 54, 2786-2801.	5.4	11
3	A 65-nm CMOS Wideband TDD Front-End With Integrated T/R Switching via PA Re-Use. IEEE Journal of Solid-State Circuits, 2017, 52, 1768-1782.	5.4	8
4	A Real-Time, 1.89-GHz Bandwidth, 175-kHz Resolution Sparse Spectral Analysis RISC-V SoC in 16-nm FinFET. IEEE Journal of Solid-State Circuits, 2019, 54, 1993-2008.	5.4	5
5	A Real-Time, Analog/Digital Co-Designed 1.89-GHz Bandwidth, 175-kHz Resolution Sparse Spectral Analysis RISC-V SoC in 16-nm FinFET. , 2018, , .		4
6	ACED. , 2018, , .		4
7	A 0.37mm2 LTE/Wi-Fi compatible, memory-based, runtime-reconfigurable 2n3m5k FFT accelerator integrated with a RISC-V core in 16nm FinFET. , 2017, , .		3