Cheng Zhuo

List of Publications by Year
in descending order

74 papers	897 citations	567281 15 h-index	580821 25 g-index
74 all docs	74 docs citations	74 times ranked	458 citing authors

#	Article	IF	Citations
1	FeCAM: A Universal Compact Digital and Analog Content Addressable Memory Using Ferroelectric. IEEE Transactions on Electron Devices, 2020, 67, 2785-2792.	3.0	75
2	Noise-Aware DVFS for Efficient Transitions on Battery-Powered IoT Devices. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 1498-1510.	2.7	62
3	On the Efficacy of Through-Silicon-Via Inductors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1322-1334.	3.1	59
4	Power Grid Analysis and Optimization Using Algebraic Multigrid. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 738-751.	2.7	45
5	From Layout to System: Early Stage Power Delivery and Architecture Co-Exploration. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1291-1304.	2.7	41
6	Novel Through-Silicon-Via Inductor-Based On-Chip DC-DC Converter Designs in 3D ICs. ACM Journal on Emerging Technologies in Computing Systems, 2014, 11, 1-14.	2.3	37
7	RCoNet: Deformable Mutual Information Maximization and High-Order Uncertainty-Aware Learning for Robust COVID-19 Detection. IEEE Transactions on Neural Networks and Learning Systems, 2021, 32, 3401-3411.	11.3	35
8	Energy-Efficient Real-Time UAV Object Detection on Embedded Platforms. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3123-3127.	2.7	29
9	Senputing: An Ultra-Low-Power Always-On Vision Perception Chip Featuring the Deep Fusion of Sensing and Computing. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 232-243.	5.4	28
10	Eva-CiM: A System-Level Performance and Energy Evaluation Framework for Computing-in-Memory Architectures. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 5011-5024.	2.7	27
11	Through-silicon-via inductor: Is it real or just a fantasy?. , 2014, , .		24
12	A novel analytic approach for outcome prediction in diffuse large B-cell lymphoma by [18F]FDG PET/CT. European Journal of Nuclear Medicine and Molecular Imaging, 2022, 49, 1298-1310.	6.4	22
13	Process Variation and Temperature-Aware Full Chip Oxide Breakdown Reliability Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1321-1334.	2.7	20
14	A deep learning framework for 18F-FDG PET imaging diagnosis in pediatric patients with temporal lobe epilepsy. European Journal of Nuclear Medicine and Molecular Imaging, 2021, 48, 2476-2485.	6.4	20
15	A Multi-Level-Optimization Framework for FPGA-Based Cellular Neural Network Implementation. ACM Journal on Emerging Technologies in Computing Systems, 2018, 14, 1-17.	2.3	19
16	A statistical approach for full-chip gate-oxide reliability analysis. , 2008, , .		18
17	Single-Inductorâ€“Multiple-Tier Regulation: TSV-Inductor-Based On-Chip Buck Converters for 3-D IC Power Delivery. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2305-2316.	3.1	18
18	A silicon-validated methodology for power delivery modeling and simulation. , 2012, , .		17

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19	Floating Random Walk-Based Capacitance Simulation Considering General Floating Metals. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1711-1715.	2.7	16
20	Countering variations and thermal effects for accurate optical neural networks. , 2020, , .		16
21	Optimally approximated and unbiased floating-point multiplier with runtime configurability. , 2020, , .		16
22	On the Reliability of In-Memory Computing: Impact of Temperature on Ferroelectric TCAM. , 2021, , .		15
23	DeU-Net 2.0: Enhanced deformable U-Net for 3D cardiac cine MRI segmentation. Medical Image Analysis, 2022, 78, 102389.	11.6	15
24	Dynamic Frequency Scaling Aware Opportunistic Through-Silicon-Via Inductor Utilization in Resonant Clocking. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 281-293.	2.7	14
25	Energy-Aware Designs of Ferroelectric Ternary Content Addressable Memory. , 2021, , .		13
26	Bayesian Inference Based Robust Computing on Memristor Crossbar. , 2021, , .		13
27	Opportunistic through-silicon-via inductor utilization in LC resonant clocks: Concept and algorithms. , 2014, , .		11
28	Silicon-Validated Power Delivery Modeling and Analysis on a 32-nm DDR I/O Interface. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1760-1771.	3.1	11
29	A Reconfigurable Approximate Multiplier for Quantized CNN Applications. , 2020, , .		11
30	Modeling and Benchmarking Computing-in-Memory for Design Space Exploration. , 2020, , .		11
31	A novel cross-layer framework for early-stage power delivery and architecture co-exploration. , 2016, , .		9
32	Reliable Memristor-based Neuromorphic Design Using Variation- and Defect-Aware Training. , 2021, , .		9
33	Efficient segmentation method using quantised and nonâ€linear CeNN for breast tumour classification. Electronics Letters, 2018, 54, 737-738.	1.0	8
34	Nonvolatile and Energy-Efficient FeFET-Based Multiplier for Energy-Harvesting Devices. , 2020, , .		8
35	Improving Fault Tolerance for Reliable DNN Using Boundary-Aware Activation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3414-3425.	2.7	8
36	Application of Deep Learning in Back-End Simulation: Challenges and Opportunities. , 2022, , .		8

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37	ICCAD Tutorial Session Paper Ferroelectric FET Technology and Applications: From Devices to Systems. , 2021, , .		8
38	A Cross-Layer Approach for Early-Stage Power Grid Design and Optimization. ACM Journal on Emerging Technologies in Computing Systems, 2015, 12, 1-20.	2.3	7
39	Modeling and optimization of magnetic core TSV-inductor for on-chip DC-DC converter. , 2018, , .		7
40	Brain metabolic characteristics distinguishing typical and atypical benign epilepsy with centro-temporal spikes. European Radiology, 2021, 31, 9335-9345.	4.5	7
41	Early-Stage Power Grid Design. , 2014, , .		5
42	Electrical-thermal co-analysis of through silicon via with equivalent circuit model. , 2017, , .		5
43	A Multicore Chip Load Model for PDN Analysis Considering Voltageâ€“Current-Timing Interdependency and Operation Mode Transitions. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019, 9, 1669-1679.	2.5	5
44	Computing-In-Memory Using Ferroelectrics: From Single- to Multi-Input Logic. IEEE Design and Test, 2022, 39, 56-64.	1.2	5
45	Optimizing the Energy Efficiency of Power Supply in Heterogeneous Multicore Chips with Integrated Switched-Capacitor Converters. , 2019, , .		4
46	Magnetic Core TSV-Inductor Design and Optimization for On-chip DC-DC Converter. ACM Transactions on Design Automation of Electronic Systems, 2022, 27, 1-23.	2.6	4
47	LIAS: A Lightweight Incentive Authentication Scheme for Forensic Services in IoV. IEEE Transactions on Automation Science and Engineering, 2023, 20, 805-820.	5.2	4
48	A Resource-Efficient Deep Learning Framework for Low-Dose Brain Pet Image Reconstruction and Analysis. , 2022, , .		4
49	Modeling, optimization and control of rotary traveling-wave oscillator. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	3
50	A Statistical Framework for Post-Fabrication Oxide Breakdown Reliability Prediction and Management. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 630-643.	2.7	3
51	A Reconfigurable Multiplier for Signed Multiplications with Asymmetric Bit-Widths. ACM Journal on Emerging Technologies in Computing Systems, 2021, 17, 1-16.	2.3	3
52	Fast Decap Allocation Based on Algebraic Multigrid. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	2
53	Novel LC resonant clocking for 3D IC using TSV-inductor and capacitor. , 2017, , .		2
54	A Cross-Layer Framework for Temporal Power and Supply Noise Prediction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1914-1927.	2.7	2

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55	Cross-layer Design for Computing-in-Memory. , 2021, , .		2
56	CN-SIM: A cycle-accurate full system power delivery noise simulator. , 2017, , .		1
57	TSV inductor optimization and its design implication. , 2017, , .		1
58	A physics-aware methodology for equivalent circuit model extraction of TSV-inductors. The Integration VLSI Journal, 2018, 63, 160-166.	2.1	1
59	Early-Stage Planning of Switched-Capacitor Converters in a Heterogeneous Chip. IEEE Access, 2020, 8, 85900-85911.	4.2	1
60	Robustness of Neuromorphic Computing with RRAM-based Crossbars and Optical Neural Networks. , 2021, , .		1
61	ANT-UNet: Accurate and Noise-Tolerant Segmentation for Pathology Image Processing. ACM Journal on Emerging Technologies in Computing Systems, 2022, 18, 1-17.	2.3	1
62	OPACT: Optimization of Approximate Compressor Tree for Approximate Multiplier. , 2022, , .		1
63	In-package P/G planes analysis and optimization based on transmission matrix method. Journal of Zhejiang University: Science A, 2008, 9, 849-857.	2.4	0
64	A cross-layer framework for early-stage full chip oxide breakdown reliability analysis. , 2016, , .		0
65	A Low-Computational Complexity System for EEG Signals Compression and Classification. , 2019, , .		0
66	Power Delivery Resonant Virus: Concept and Applications. , 2019, , .		0
67	Revisiting EAVP for Power Delivery Decoupling Optimization. , 2019, , .		0
68	The Impact of Emerging Technologies on Architectures and System-level Management: Invited Paper. , 2019, , .		0
69	Joint Sparsity with Mixed Granularity for Efficient GPU Implementation. , 2021, , .		0
70	Impact of Supply Noise on Nano-Meter VLSI Design: Hard or Soft Threshold?. , 2021, , .		0
71	A Physical-Aware Framework for Memory Network Design Space Exploration. , 2021, , .		0
72	Earlyâ€stage microfluidic network design framework using graph sparsificiation based optimisation. Electronics Letters, 2019, 55, 1034-1037.	1.0	0

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73	Analog Content Addressable Memory using Ferroelectric: A Case Study of Search-in-Memory. , 2020, , .		0
74	VirtualSync+: Timing Optimization with Virtual Synchronization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, , 1-1.	2.7	0