John WILLIAMS

List of Publications by Year in descending order

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	1937685	2053705
322	4	5
citations	h-index	g-index
32	32	287
docs citations	times ranked	citing authors
	citations 32	322 4 citations h-index 32 32

#	Article	IF	CITATIONS
1	Simultaneous Registration of Multiple Corresponding Point Sets. Computer Vision and Image Understanding, 2001, 81, 117-142.	4.7	79
2	The correspondence framework for 3D surface matching algorithms. Computer Vision and Image Understanding, 2005, 97, 347-383.	4.7	47
3	FPGA-based cloud detection for real-time onboard remote sensing. , 0, , .		23
4	Reconfigurable FPGAS for real time image processing in space., 0,,.		20
5	On-board satellite image compression using reconfigurable FPGAs. , 0, , .		17
6	FIFO Communication Models in Operating Systems for Reconfigurable Computing., 0,,.		13
7	Correspondence-Free Determination of the Affine Fundamental Matrix. IEEE Transactions on Pattern Analysis and Machine Intelligence, 2007, 29, 82-97.	13.9	13
8	Automatic Self-Reconfiguration of System-on-Chip Peripherals. , 2007, , .		13
9	A Reconfigurable Cluster-on-Chip Architecture with MPI Communication Layer. , 2006, , .		12
10	FPGA Based Satellite Adaptive Image Compression System. Journal of Aerospace Engineering, 2003, 16, 129-137.	1.4	9
11	The Egret platform for reconfigurable system on chip. , 0, , .		8
12	Design Exploration for FPGA-Based Multiprocessor Architecture: JPEG Encoding Case Study., 2009,,.		8
13	Simultaneous registration of multiple point sets using orthonormal matrices. , 0, , .		7
14	Asymmetric Multi-Processor Architecture for Reconfigurable System-on-Chip and Operating System Abstractions., 2007,,.		7
15	A 3D acquisition and modelling system. , 0, , .		6
16	FPGA based real-time adaptive filtering for space applications. , 0, , .		6
17	A Hybrid Reconfigurable Cluster-on-Chip Architecture with Message Passing Interface for Image Processing Applications., 2007,,.		5
18	Global 3D rigid registration of medical images. , 2000, , .		4

#	Article	IF	Citations
19	Multi Stream Cipher Architecture for Reconfigurable System-on-Chip. , 2006, , .		4
20	An ILP formulation for architectural synthesis and application mapping on FPGA-based hybrid multi-processor SOC., 2008,,.		4
21	A catalog of hardware acceleration techniques for real-time reconfigurable system on chip. , 0, , .		3
22	A non-linear filtering approach to image matching. , 0, , .		2
23	Evaluation of a novel multiple point set registration algorithm. , 0, , .		2
24	Flexible real time signal filtering in space using reconfigurable logic. , 0, , .		2
25	Egret: a platform for a reconfigurable system-on-chip. , 2004, , .		2
26	System Level Design Methodology for Hybrid Multi-Processor SoC on FPGA. , 2008, , .		2
27	Multiple view surface registration with error modeling and analysis. , 0, , .		2
28	A real-time asymmetric multiprocessor reconfigurable system-on-chip architecture., 2005, 6035, 49.		1
29	Synthesising surface matching algorithms using the correspondence framework. Pattern Recognition and Image Analysis, 2007, 17, 199-203.	1.0	1
30	An extended Kalman filtering approach to high precision stereo image matching. , 0, , .		0
31	Dynamic loading of peripherals on reconfigurable system-on-chip. , 2005, , .		O
32	VPN Acceleration Using Reconfigurable System-On-Chip Technology. , 2006, , .		0