Chua-Chin Wang

List of Publications by Year
in descending order

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280	1,682	448610	536525
papers	citations	19 h-index	29 g-index

280	280	280	1033
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Single-chip DCâ€“DC buck converter design based on PWM with high-efficiency in light load. International Journal of Electronics Letters, 2023, 11, 255-266.	0.7	0
2	A 100-MHz 3.352-mW 8-bit shift register using low-power DETFF using 90-nm CMOS process. International Journal of Electronics Letters, 2023, 11, 300-315.	0.7	2
3	Lightweight Deep Neural Network for Joint Learning of Underwater Object Detection and Color Conversion. IEEE Transactions on Neural Networks and Learning Systems, 2022, 33, 6129-6143.	7.2	66
4	2$$imes $$VDD 500ÂMHz Digital Output Buffer with Optimal Driver Transistor Sizing for Slew Rate Self-adjustment and Leakage Reduction Using 28-nm CMOS Process. Circuits, Systems, and Signal Processing, 2021, 40, 2824-2840.	1.2	2
5	Tutorial: Design of High-Speed Nano-Scale CMOS Mixed-Voltage Digital I/O Buffer With High Reliability to PVTL Variations. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 562-567.	2.2	2
6	A 40-nm CMOS Piezoelectric Energy Harvesting IC for Wearable Biomedical Applications. Electronics (Switzerland), 2021, 10, 649.	1.8	4
7	High-Accuracy Impedance Read-out Circuit for BIA-type Biomedical Sensors. Circuits, Systems, and Signal Processing, 2021, 40, 4187-4195.	1.2	0
8	SRAM-based Computation In Memory Architecture to Realize Single Command of Add-Multiply Operation and Multifunction. , 2021, , .		0
9	67.5-fJ Per Access 1-kb SRAM Using 40-nm Logic CMOS Process. , 2021, , .		3
10	High Resolution Time-to-Digital Converter Design with Anti-PVT-Variation Mechanism. , 2021, , .		3
11	0.7 % error rate 3A bidirectional current sensor using high voltage CMOS process. Microelectronics Journal, 2021, 114, 105127.	1.1	2
12	200-MHz Single-Ended 6T 1-kb SRAM With 0.2313 pJ Energy/Access Using 40-nm CMOS Logic Process. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3163-3166.	2.2	4
13	A 40-nm CMOS Multifunctional Computing-in-Memory (CIM) Using Single-Ended Disturb-Free 7T 1-Kb SRAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 2172-2185.	2.1	3
14	On-chip CMOS Corner Detector Design for Panel Drivers*. , 2021, , .		2
15	A Single-Ended Low Power 16-nm FinFET 6T SRAM Design With PDP Reduction Circuit. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3478-3482.	2.2	5
16	An adaptive constant current and voltage mode P&O-based Maximum Power Point Tracking controller IC using 0.5-<mml:math xmlns:mml="http://www.w3.org/1998/Math/MathML" display="inline" id="d1e1377" altimg="si3.svg"><mml:mrow><mml:mi mathvariant="normal">Î¼</mml:mi><mml:mi mathvariant="normal">m</mml:mi></mml:mrow></mml:math> HV CMOS. Microelectronics Journal, 2021, 118, 105295.	1.1	7
17	A 2.5-GHz 2Ã—VDD 16-nm FinFET Digital Output Buffer with Slew Rate and Duty Cycle Self-Adjustment. , 2021, , .		1
18	Power-effective ROM-less DDFS Design Approach with High SFDR Performance. Journal of Signal Processing Systems, 2020, 92, 213-224.	1.4	1

#	Article	IF	Citations
19	A Single-Ended 28-nm CMOS 6T SRAM Design with Read-assist Path and PDP Reduction Circuitry. Journal of Circuits, Systems and Computers, 2020, 29, 2050095.	1.0	3
20	Anti-PVT-Variation Low-Power Time-to-Digital Converter Design Using 90-nm CMOS Process. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2069-2073.	2.1	12
21	A Slew Rate Enhanced 2 x VDD I/O Buffer With Precharge Timing Technique. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2707-2711.	2.2	4
22	2-GHz 2Ã—VDD 28-nm CMOS Digital Output Buffer with Slew Rate Auto-Adjustment Against Process and Voltage Variations. Journal of Circuits, Systems and Computers, 2020, 29, 2050088.	1.0	1
23	Multifunctional In-Memory Computation Architecture Using Single-Ended Disturb-Free 6T SRAM. Lecture Notes in Electrical Engineering, 2020, , 49-57.	0.3	4
24	A Slew Rate Variation Compensated <inline-formula> <tex-math notation="LaTeX">$2imes$ </tex-math> </inline-formula>VDD I/O Buffer Using Deterministic P/N-PVT Variation Detection Method. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 116-120.	2.2	11
25	A PVT Validation Phase-Lock Loop with Multi-Band VCO Applied in Closed-Loop FOGs. , 2019, , .		1
26	74-dBc SFDR 71-MHz Four-Stage Pipeline ROM-Less DDFS Using Factorized Second-Order Parabolic Equations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2464-2468.	2.1	4
27	A 1.5A 88.6% Li-ion Battery Charger Design using Pulse Swallow Technique in Light Load. , 2019, , .		2
28	Ultra Low Power Single-ended 6T SRAM Using 40 nm CMOS Technology. , 2019, , .		5
29	High Efficiency Buck Converter with Wide Load Current Range using Dual-Mode of PWM and PSM. , 2019, , .		8
30	Temperature-to-Frequency Converter With 1.47% Error Using Thermistor Linearity Calibration. IEEE Sensors Journal, 2019, 19, 4804-4811.	2.4	6
31	A Broken Line Detection Circuit for Multi-cell Li-ion Battery Module1. , 2019, , .		0
32	2.5 GHz Data Rate 2 Ã— VDD Digital Output Buffer Design Realized by 16-nm FinFET CMOS. , 2019, , .		2
33	Small RV-Based Deep-Towed Seafloor Sampling Systems. , 2019, , .		0
34	500 MHz 90 nm CMOS 2Â $$imes $$ Ã— ÂVDD Digital Output Buffer Immunity to Process and Voltage Variations. Circuits, Systems, and Signal Processing, 2019, 38, 556-568.	1.2	5
35	56.67 fJ/bit single-ended disturb-free 5T loadless 4 kb SRAM using 90 nm CMOS technology. Analog Integrated Circuits and Signal Processing, 2018, 96, 435-443.	0.9	2
36	A Lock Detector Loop for Low-power PLL-Based Clock and Data Recovery Circuits. Circuits, Systems, and Signal Processing, 2018, 37, 1692-1703.	1.2	4

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37	40-nm 2Ã—VDD Digital Output Buffer Design With DDR4-Compliant Slew Rate. , 2018, , .		2
38	High SFDR Pipeline ROM-less DDFS Design on FPGA Platform Using Parabolic Equations. , 2018, , .		1
39	Switching Activity Analysis of Shifters and Multipliers for Application to ROM-less DDFS Architecture Selection for Low Power Performance. , 2018, , .		0
40	A High-Precision CMOS Temperature Sensor with Thermistor Linear Calibration in the (â^'5 Â°C, 120 Â°C) Temperature Range. Sensors, 2018, 18, 2165.	2.1	8
41	A 90-nm CMOS 800 MHz 2 $$imes$$ Ã— VDD output buffer with leakage detection and output current self-adjustment. Analog Integrated Circuits and Signal Processing, 2018, 97, 343-350.	0.9	6
42	2 Ã— VDD output buffer with 36.4% slew rate improvement using leakage current compensation. Electronics Letters, 2017, 53, 62-64.	0.5	7
43	State of charge, state of health, and state of function monitoring for EV BMS. , 2017, , .		12
44	A 19.38 dBm OIP3 gm-boosted up-conversion CMOS mixer for 5â€“6 GHz application. Microelectronics Journal, 2017, 60, 38-44.	1.1	8
45	A Dynamic Leakage and Slew Rate Compensation Circuit for 40-nm CMOS Mixed-Voltage Output Buffer. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 3166-3174.	2.1	7
46	A readout circuit with cell output slew rate compensation for 5T single-ended 28Ânm CMOS SRAM. Microelectronics Journal, 2017, 70, 107-116.	1.1	7
47	$2imesext{VDD}$ 40-nm CMOS Output Buffer With Slew Rate Self-Adjustment Using Leakage Compensation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 812-816.	2.2	6
48	A primary-side output current estimator with process compensator for flyback LED drivers. , 2017, , .		0
49	2xVDD digital output buffer insensitive to process and voltage variations. , 2017, , .		2
50	High-voltage bidirectional current sensor. , 2017, , .		3
51	Highly Sensitive FPW-Based Microsystem for Rapid Detection of Tetrahydrocannabinol in Human Urine. Sensors, 2017, 17, 2760.	2.1	6
52	A pipeline ROM-less DDFS using equal-division interpolation. , 2017, , .		1
53	Dynamic power estimation for ROM-less DDFS designs using switching activity analysis. , 2017, , .		2
54	A novel frequency-shift readout system for CEA concentration detection application. , 2016, , .		2

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55	Disturb-free 5T loadless SRAM cell design with multi-vth transistors using 28 nm CMOS process. , 2016, , .		3
56	A flyback driver with adaptive switching frequency control for smart lighting1. , 2016, , .		0
57	A method of leakage reduction and slew-rate adjustment in 2Ã—VDD output buffer for 28 nm CMOS technology and above. , 2016, , .		3
58	On-chip accurate primary-side output current estimator for flyback LED driver control. , 2016, , .		2
59	Highâ€voltage onâ€chip current sensor design and analysis for battery modules. IET Circuits, Devices and Systems, 2016, 10, 492-496.	0.9	1
60	A Leakage Compensation Design for Low Supply Voltage SRAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1761-1769.	2.1	18
61	Analysis of Calibrated On-Chip Temperature Sensor With Process Compensation for HV Chips. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 217-221.	2.2	5
62	A capacity monitoring system with HV current sensor and calibrated current estimation approach. , 2015, , .		4
63	A high-speed 2×VDD output buffer with PVTL detection using 40-nm CMOS technology. , 2015, , .		3
64	A Â±3.07% frequency variation clock generator implemented using HV CMOS process. Microelectronics Journal, 2015, 46, 285-290.	1.1	2
65	A 60 V Tolerance Transceiver With ESD Protection for FlexRay-Based Communication Systems. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 752-760.	3.5	5
66	A wide range and high conversion gain power detector for frequency shift sensing applications. , 2015, , .		0
67	A 30V rail-to-rail operational amplifier. Microelectronics Journal, 2015, 46, 911-915.	1.1	0
68	Wide-range CTAT and PTAT sensors with second-order calibration for on-chip thermal monitoring. Microelectronics Journal, 2015, 46, 819-824.	1.1	0
69	Process corner detection by skew inverters for 500MHZ 2Ã—VDD output buffer using 40-nm CMOS technology. Microelectronics Journal, 2015, 46, 1-11.	1.1	7
70	Low power cross-domain high-voltage transmitters for battery management systems. , 2014, , .		1
71	Â±10.5 V 16â€channel programmable pulse generator using highâ€voltage BCD CMOS process. Electronics Letters, 2014, 50, 1797-1799.	0.5	2
72	An all-digital battery capacity monitor using calibrated current estimation approach. , 2014, , .		0

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73	A single-ended disturb-free 5T loadless SRAM with leakage sensor and read delay compensation using 40 nm CMOS process. , 2014, , .		6
74	A CMOS wide-range temperature sensor with process compensation and second-order calibration for Battery Management Systems. , 2014, , .		3
75	Slew rate improved 2×VDD output buffer using leakage and delay compensation. , 2014, , .		6
76	A FlexRay Transceiver Design with Bus Guardian for In-car Networking Systems Compliant with FlexRay Standard. Journal of Signal Processing Systems, 2014, 74, 221-233.	1.4	2
77	32% Slew rate and 27% data rate improved 2×VDD output buffer using PVTL compensation. , 2014, , .		3
78	Bus Driver controller with hazard detection for FlexRay protocol 3.0.1. , 2014, , .		0
79	A fast CEA analyzer prototype for point of care testing. , 2014, , .		2
80	On-Chip Process and Temperature Monitor for Self-Adjusting Slew Rate Control of 2$,imes,$VDD Output Buffers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 1432-1440.	3.5	11
81	High voltage operational amplifier and high voltage transceiver using 0.25 µm 60V BCD process for Battery Management Systems. , 2013, , .		3
82	A CEA concentration measurement system using FPW biosensors and frequency-shift readout IC. , 2013, , .		7
83	A 50-MHz clock generator with voltage and temperature compensation using low dropout regulator. , 2013, , .		2
84	A 800 Mbps and 12.37 ps Jitter Bidirectional Mixed-Voltage I/O Buffer With Dual-Path Gate-Tracking Circuit. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 116-124.	3.5	17
85	A low-power transceiver design for FlexRay-based communication systems. Microelectronics Journal, 2013, 44, 359-366.	1.1	2
86	A 2Ã—VDD output buffer with PVT detector for slew rate compensation. Microelectronics Journal, 2013, 44, 393-399.	1.1	4
87	A 10-bit 400-MS/s current-steering DAC with process calibration. , 2013, , .		1
88	A high-speed 2×VDD output buffer with PVT detection using 40-nm CMOS technology. , 2013, , .		6
89	A Protein Concentration Measurement System Using a Flexural Plate-Wave Frequency-Shift Readout Technique. Sensors, 2013, 13, 86-105.	2.1	3
90	A delay-based transceiver with over-current protection for ECU nodes in automobile FlexRay systems. , 2013, , .		2

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91	A fast FPW allergy analyzer prototype for point of care (POC). , 2012, , .		1
92	A PLC transceiver design of in-vehicle power line in FlexRay-based automotive communication systems. , 2012, , .		4
93	Feed-forward Output Swing Prediction AGC with Parallel-Detect Singular-Store Peak Detector. , 2012, , .		3
94	A slew rate self-adjusting 2×VDD output buffer With PVT compensation. , 2012, , .		4
95	A fast FPW-based protein concentration measurement system. , 2012, , .		0
96	A high voltage analog multiplexer with digital calibration for battery management systems. , 2012, , .		7
97	Configurable Active Star design for automobile FlexRay systems. , 2012, , .		0
98	On-chip MOS PVT variation monitor for slew rate self-adjusting 2×VDD output buffers. , 2012, , .		6
99	Single-ended disturb-free 5T loadless SRAM Cell using 90 nm CMOS process. , 2012, , .		2
100	A Battery Interconnect Module with high voltage transceiver using 0.25 µm 60V BCD process for Battery Management Systems. , 2012, , .		5
101	A Single-Chip 60-V Bulk Charger for Series Li-Ion Batteries With Smooth Charge-Mode Transition. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 1588-1597.	3.5	22
102	A reconfigurable 16-channel HV stimulator ASIC for Spinal Cord Stimulation systems. , 2012, , .		7
103	Linear programmable gain amplifier using reconfiguration local-feedback transconductors. , 2012, , .		1
104	Feed-forward Output Swing Prediction AGC design with Parallel-Detect Singular-Store Peak Detector. Microelectronics Journal, 2012, 43, 250-256.	1.1	4
105	A low power 48-dB/stage linear-in-dB variable gain amplifier for direct-conversion receivers. Microelectronics Journal, 2012, 43, 274-279.	1.1	5
106	A Signed Array Multiplier with Bypassing Logic. Journal of Signal Processing Systems, 2012, 66, 87-92.	1.4	3
107	ROM-less DDFS using non-equal division parabolic polynomial interpolation method. , 2011, , .		5
108	A 48-dB dynamic gain range/stage linear-in-dB low power Variable Gain Amplifier for direct-conversion receivers. , 2011, , .		6

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109	On-chip process and temperature compensation and self-adjusting slew rate control for output buffer. , 2011, , .		2
110	2.45 GHz ZigBee receiver frontend for HAN with smart meter. , 2011, , .		0
111	A high speed transceiver front-end design with fault detection for FlexRay-based automotive communication systems. , 2011, , .		3
112	A high voltage battery charger with smooth charge mode transition in BCD process. , 2011, , .		7
113	A Wide Voltage Range Digital I/O Design Using Novel Floating N-Well Circuit. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1481-1485.	2.1	5
114	One-Time-Implantable Spinal Cord Stimulation System Prototype. IEEE Transactions on Biomedical Circuits and Systems, 2011, 5, 490-498.	2.7	27
115	A ROM-less DDFS Based on a Parabolic Polynomial Interpolation Method with an Offset. Journal of Signal Processing Systems, 2011, 64, 351-359.	1.4	7
116	A high-efficiency DCâ€“DC buck converter for sub-2Ã—VDD power supply. Microelectronics Journal, 2011, 42, 709-717.	1.1	10
117	A high precision low dropout regulator with nested feedback loops. Microelectronics Journal, 2011, 42, 966-971.	1.1	6
118	A frequency-shift readout system for FPW allergy biosensor. , 2011, , .		8
119	20 MHz accurate peak detector for FPW allergy biosensor with digital calibration. , 2011, , .		3
120	A low power wake up detector for ECU nodes in an automobile flexray system. , 2011, , .		2
121	Domestic Indirect Feedback Compensation of multiple-stage amplifiers for multiple-voltage level-converting amplification. , 2011, , .		4
122	One-Time Implantable SCS System. , 2011, , .		2
123	Low power RC5 cipher for ZigBee portable biomedical systems. , 2011, , .		2
124	A fast-locking clock and data recovery circuit with a lock detector loop. , 2011, , .		3
125	Ultrasonic transcutaneous energy transfer using a continuous wave 650kHz Gaussian shaded transmitter. Ultrasonics, 2010, 50, 666-674.	2.1	81
126	A linear LDO regulator with modified NMCF frequency compensation independent of off-chip capacitor and ESR. Analog Integrated Circuits and Signal Processing, 2010, 63, 239-244.	0.9	3

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127	Energy-Efficient Double-Edge Triggered Flip-Flop. Journal of Signal Processing Systems, 2010, 61, 347-352.	1.4	2
128	A low-power 2.45GHz WPAN modulator/demodulator. Microelectronics Journal, 2010, 41, 150-154.	1.1	4
129	A one-time implantable wireless power bidirectional transmission spinal cord stimulation system. , 2010, , .		5
130	A high precision low dropout regulator with nested feedback loops. , 2010, , .		2
131	All-Digital Frequency Synthesizer Using a Flying Adder. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 597-601.	2.2	10
132	0.9 V to 5 V Bidirectional Mixed-Voltage I/O Buffer With an ESD Protection Output Stage. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 612-616.	2.2	12
133	Self-Sampled All-MOS ASK Demodulator for Lower ISM Band Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 265-269.	2.2	40
134	$(1/3) imes hbox{VDD}$-to- $(3/2) imes hbox{VDD}$ Wide-Range I/O Buffer Using 0.35- $muhbox{m}$ 3.3-V CMOS Technology. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 126-130.	2.2	3
135	A Self-Disabled Sensing Technique for Content-Addressable Memories. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 31-35.	2.2	34
136	A high-efficiency DC-DC buck converter for sub-3×VDD power supply. , 2010, , .		0
137	A 125-MHz wide-range mixed-voltage I/O buffer using gated Floating N-well circuit. , 2010, , .		0
138	A $1/2 imes {hbox {VDD}}$ to $3 imes {hbox {VDD}}$ Bidirectional I/O Buffer With a Dynamic Gate Bias Generator. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 1642-1653.	3.5	14
139	450 MHz 1.0 V to 1.8 V bidirectional mixed-voltage I/O buffer using 90-nm process. , 2010, , .		1
140	A Transceiver Front End for Electronic Control Units in FlexRay-Based Automotive Communication Systems. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 460-470.	3.5	16
141	A mini-invasive multi-function biomedical pressure measurement system ASIC. , 2010, , .		2
142	A PCI166-compatible 3×VDD-tolerant mixed-voltage I/O buffer. , 2010, , .		1
143	On the capacitively coupled transmission channel for body network application. , 2010, , .		1
144	A highâ€SFDR direct digital frequency synthesizer with embedded errorâ€compensation CMOS OTP ROM for wireless receivers. Microwave and Optical Technology Letters, 2009, 51, 1695-1699.	0.9	1

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145	High-PSR sync separator for TV signals. Analog Integrated Circuits and Signal Processing, 2009, 61, 279-286.	0.9	0
146	Low-Power Multiplier Design Using a Bypassing Technique. Journal of Signal Processing Systems, 2009, 57, 331-338.	1.4	14
147	Wide-Range 5.0/3.3/1.8-V I/O Buffer Using 0.35-<spl mu>m 3.3-V CMOS Technology. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 763-772.	3.5	15
148	Physical layer design for ECU nodes in FlexRay-based automotive communication systems. , 2009, , .		3
149	Low-power 7.2 GHz complementary all-N-transistor logic using 90 nm CMOS technology. , 2009, , .		4
150	A 0.9 V to 5 V mixed-voltage I/O buffer using NMOS clamping technique. , 2009, , .		2
151	Baseband Receiver Design for the MBOA Ultra Wideband Wireless Personal Area Networks. IEICE Transactions on Communications, 2009, E92-B, 143-149.	0.4	0
152	Power-Aware Design of An 8-Bit Pipelining ANT-Based CLA Using Data Transition Detection. Journal of Signal Processing Systems, 2008, 52, 127-135.	1.4	4
153	A CMOS optoâ€electronic single chip using the hybrid scheme for optical receivers. Microwave and Optical Technology Letters, 2008, 50, 2430-2434.	0.9	0
154	A 570-kbps ASK demodulator without external capacitors for low-frequency wireless bio-implants. Microelectronics Journal, 2008, 39, 130-136.	1.1	9
155	A low-power ADPLL using feedback DCO quarterly disabled in time domain. Microelectronics Journal, 2008, 39, 832-840.	1.1	10
156	A single-chip CMOS IF-band converter design for DVB-T receivers. Microelectronics Journal, 2008, 39, 117-129.	1.1	1
157	A Li-ion battery charging design for biomedical implants. , 2008, , .		5
158	All-MOS ASK Demodulator for Low-Frequency Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 474-478.	2.2	28
159	70 dB Dynamic Range CMOS Wideband Digital Variable Gain Amplifier for AGC in DVB-T/H Receivers. Circuits, Systems, and Signal Processing, 2008, 27, 367-379.	1.2	5
160	1.8 V to 5.0 V mixed-voltage-tolerant I/O buffer with 54.59% output duty cycle. , 2008, , .		3
161	A power-aware 2-dimensional bypassing multiplier using cell-based design flow. , 2008, , .		11
162	A Mini-Invasive Long-Term Bladder Urine Pressure Measurement ASIC and System. IEEE Transactions on Biomedical Circuits and Systems, 2008, 2, 44-49.	2.7	43

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163	A Low Power High-Speed 8-Bit Pipelining CLA Design Using Dual-Threshold Voltage Domino Logic. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 594-598.	2.1	19
164	A System Prototype for Portable Wireless Medical Devices. , 2008, , .		1
165	Mixed-voltage I/O buffer using 0.35 μm CMOS technology. , 2008, , .		1
166	R-less and C-less self-sampled ASK demodulator for lower ISM band applications. , 2008, , .		2
167	A ROM-less DDFS using a nonlinear DAC with an error compensation current array. , 2008, , .		1
168	A self-disable sense technique with differential NAND cell for content-addressable memories. , 2008, , .		2
169	Bus Guardian Design for automobile networking ecu nodes compliant with FlexRay standards. , 2008, , .		8
170	A mini-invasive multi-function bladder urine pressure measurement system. , 2008, , .		1
171	A ROM-less direct digital frequency synthesizer based on 16-segment parabolic polynomial interpolation. , 2008, , .		3
172	A 1.7-ns ACCESS TIME SRAM USING VARIABLE BULK BIAS WORDLINE-CONTROLLED TRANSISTORS. Journal of Circuits, Systems and Computers, 2008, 17, 943-956.	1.0	3
173	Power-saving nano-scale DRAMs with an adaptive refreshing clock generator. , 2008, , .		0
174	A Transceiver Design for Electronic Control Unit (ECU) Nodes in FlexRay-based Automotive Communication Systems. , 2008, , .		2
175	A 32-bit carry lookahead adder design using complementary all-N-transistor logic. , 2008, , .		2
176	ZigBee 868/915-MHz Modulator/Demodulator for Wireless Personal Area Network. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 936-939.	2.1	20
177	A Phase-Locked Loop with 30% Jitter Reduction Using Separate Regulators. VLSI Design, 2008, 2008, 1-8.	0.5	1
178	A Low-power Sensorless Inverter Controller of Brushless DC Motors. , 2007, , .		5
179	An Implantable Long-term Bladder Urine Pressure Measurement System with a 1-atm Canceling Instrumentation Amplifier. , 2007, , .		5
180	Mixed-voltage-tolerant I/O buffer using a clamping dynamic gate bias generator. , 2007, , .		1

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181	A Low-Power 2.45 GHz ZigBee Transceiver for Wearable Personal Medical Devices in WPAN. , 2007, , .		17
182	Mixed-Voltage-Tolerant I/O Buffer Design. , 2007, , .		1
183	C-less and R-less Low-Frequency ASK Demodulator for Wireless Implantable Devices. , 2007, , .		9
184	A 4-kb Low-Power SRAM Design With Negative Word-Line Scheme. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 1069-1076.	0.1	32
185	A Low Power DDFS Design with Error Compensation Using A Nonlinear Digital-to-Analog Converter. , 2007, , .		2
186	Handheld DVB-T Digital TV with An Automatic Antenna Selection Method for Mobile Reception. , 2007, , .		8
187	A Direct Digital Frequency Synthesizer with CMOS OTP ROMÂ§. , 2007, , .		0
188	DVB-T Receiver With a Fully Digital I/Q Separator. , 2007, , .		0
189	Voltage-to-frequency converter with high sensitivity using all-MOS voltage window comparator. Microelectronics Journal, 2007, 38, 197-202.	1.1	16
190	An 80MHz PLL with 72.7ps peak-to-peak jitter. Microelectronics Journal, 2007, 38, 716-721.	1.1	3
191	An All-MOS High Linearity Voltage-to-Frequency Converter Chip with 520 KHz/V Sensitivity. , 2006, , .		6
192	A low-power 2D bypassing multiplier using 0.35 μm CMOS technology. , 2006, , .		4
193	Codec Design for Variable-Length to Fixed-Length Data Conversion for H.263. , 2006, , .		0
194	High-sensitivity and high-mobility compact DVB-T receiver for in-car entertainment. IEEE Transactions on Consumer Electronics, 2006, 52, 21-25.	3.0	5
195	A Linear LDO Regulator with Modified NMCF Frequency Compensation Independent of Off-chip Capacitor and ESR. , 2006, , .		10
196	Clock-and-Data Recovery Design for LVDS Transceiver Used in LCD Panels. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2006, 53, 1318-1322.	2.3	8
197	An Implantable SOC Chip for Micro-stimulating and Neural Signal Recording. , 2006, , .		0
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