Antonio G M Strollo

List of Publications by Year
in descending order

52 papers	1,303 citations	430874 18 h-index	377865 34 g-index
52 all docs	52 docs citations	52 times ranked	758 citing authors

#	Article	IF	Citations
1	Approximate Multipliers Based on New Approximate Compressors. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 4169-4182.	5.4	171
2	Comparison and Extension of Approximate 4-2 Compressors for Low-Power Approximate Multipliers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3021-3034.	5.4	141
3	A 1.27 GHz, All-Digital Spread Spectrum Clock Generator/Synthesizer in 65 nm CMOS. IEEE Journal of Solid-State Circuits, 2010, 45, 1048-1060.	5.4	128
4	Truncated Binary Multipliers With Variable Correction and Minimum Mean Square Error. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 1312-1325.	5.4	96
5	Design of Fixed-Width Multipliers With Linear Compensation Function. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 947-960.	5.4	57
6	Variable Latency Speculative Parallel Prefix Adders for Unsigned and Signed Operands. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1200-1209.	5.4	47
7	Efficient Logarithmic Converters for Digital Signal Processing Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 667-671.	3.0	44
8	Fixed-Width Multipliers and Multipliers-Accumulators With Min-Max Approximation Error. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 2375-2388.	5.4	44
9	A 630 MHz, 76 mW Direct Digital Frequency Synthesizer Using Enhanced ROM Compression Technique. IEEE Journal of Solid-State Circuits, 2007, 42, 350-360.	5.4	43
10	High Speed Speculative Multipliers Based on Speculative Carry-Save Tree. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 3426-3435.	5.4	42
11	A 380 MHz Direct Digital Synthesizer/Mixer With Hybrid CORDIC Architecture in 0.25 $mu{hbox {m}}$ CMOS. IEEE Journal of Solid-State Circuits, 2007, 42, 151-160.	5.4	40
12	Reducing Lookup-Table Size in Direct Digital Frequency Synthesizers Using Optimized Multipartite Table Method. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 2116-2127.	5.4	40
13	High-Performance Special Function Unit for Programmable 3-D Graphics Processors. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 1968-1978.	5.4	40
14	Low-power approximate MAC unit. , 2017, , .		34
15	Direct Digital Frequency Synthesizer Using Nonuniform Piecewise-Linear Approximation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2409-2419.	5.4	25
16	A 2.5-GHz DDFS-PLL With 1.8-MHz Bandwidth in 0.35-mum CMOS. IEEE Journal of Solid-State Circuits, 2008, 43, 1403-1413.	5.4	21
17	Accurate Fixed-Point Logarithmic Converter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 526-530.	3.0	20
18	On the use of approximate adders in carry-save multiplier-accumulators. , 2017, , .		19

#	Article	IF	Citations
19	Approximate Multipliers Using Static Segmentation: Error Analysis and Improvements. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 2449-2462.	5.4	19
20	A 430 MHz, 280 mW Processor for the Conversion of Cartesian to Polar Coordinates in 0.25 $muhbox{m}$ CMOS. IEEE Journal of Solid-State Circuits, 2008, 43, 2503-2513.	5.4	18
21	An FDD Wireless Diversity Receiver With Transmitter Leakage Cancellation in Transmit and Receive Bands. IEEE Journal of Solid-State Circuits, 2018, 53, 1945-1959.	5.4	18
22	A Standard-Cell-Based All-Digital PWM Modulator With High Resolution and Spread- Spectrum Capability. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3885-3896.	5.4	18
23	Digital Synthesizer/Mixer With Hybrid CORDICâ€“Multiplier Architecture: Error Analysis and Optimization. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 364-373.	5.4	17
24	Low-Power Approximate Multiplier with Error Recovery using a New Approximate 4-2 Compressor. , 2020, , .		16
25	A 3.3 GHz Spread-Spectrum Clock Generator Supporting Discontinuous Frequency Modulations in 28 nm CMOS. IEEE Journal of Solid-State Circuits, 2015, 50, 2074-2089.	5.4	15
26	A Modified IBIS Model Aimed at Signal Integrity Analysis of Systems in Package. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 1921-1928.	5.4	14
27	Approximate Recursive Multipliers Using Low Power Building Blocks. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 1315-1330.	4.6	14
28	On the Use of Approximate Multipliers in LMS Adaptive Filters. , 2018, , .		9
29	Comparison of Sneo-Based Neural Spike Detection Algorithms for Implantable Multi-Transistor Array Biosensors. Electronics (Switzerland), 2021, 10, 410.	3.1	9
30	FPGA Implementation of Gaussian Mixture Model Algorithm for 47â€‰fps Segmentation of 1080p Video. Journal of Electrical and Computer Engineering, 2013, 2013, 1-8.	0.9	8
31	Power-precision scalable latch memories. , 2017, , .		8
32	Low-Power Hardware Implementation of Least-Mean-Square Adaptive Filters Using Approximate Arithmetic. Circuits, Systems, and Signal Processing, 2019, 38, 5606-5622.	2.0	7
33	A Low Power 1024-Channels Spike Detector Using Latch-Based RAM for Real-Time Brain Silicon Interfaces. Electronics (Switzerland), 2021, 10, 3068.	3.1	7
34	Variable latency speculative Han-Carlson adders topologies. , 2015, , .		6
35	Quality-Scalable Approximate LMS Filter. , 2018, , .		6
36	A Novel Module-Sign Low-Power Implementation for the DLMS Adaptive Filter With Low Steady-State Error. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 297-308.	5.4	6

#	Article	IF	Citations
37	A high performance floating-point special function unit using constrained piecewise quadratic approximation. , 2008, , .		5
38	Hardware Implementation of Digital Signal Processing Algorithms. Journal of Electrical and Computer Engineering, 2013, 2013, 1-2.	0.9	5
39	An Efficient Digital Background Control for Hybrid Transformer-Based Receivers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 3068-3080.	5.4	4
40	A 1.45 GHz All-Digital Spread Spectrum Clock Generator in 65nm CMOS for Synchronization-Free SoC Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3839-3852.	5.4	4
41	Real-Time Downsampling in Digital Storage Oscilloscopes With Multichannel Architectures. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 4142-4155.	5.4	4
42	Single Flip-Flop Driving Circuit for Glitch-Free NAND-Based Digitally Controlled Delay-Lines. Circuits, Systems, and Signal Processing, 2017, 36, 1341-1360.	2.0	3
43	Constrained piecewise polinomial approximation for hardware implementation of elementary functions. , 2008, , .		2
44	Design of Low-Power Approximate LMS Filters with Precision-Scalability. Lecture Notes in Electrical Engineering, 2019, , 237-243.	0.4	2
45	High-speed differential resistor ladder for A/D converters. , 2010, , .		1
46	Towards a Frequency Domain Processor for Real-Time SIFT-based Filtering. Lecture Notes in Electrical Engineering, 2016, , 161-167.	0.4	1
47	A SISO Register Circuit Tailored for Input Data with Low Transition Probability. IEEE Transactions on Computers, 2017, 66, 45-51.	3.4	1
48	Stall-Aware Fixed-Point Implementation of LMS Filters. , 2018, , .		1
49	Variable-Rounded LMS Filter for Low-Power Applications. Lecture Notes in Electrical Engineering, 2020, , 155-161.	0.4	1
50	A Novel Low-Power High-Precision Implementation for Signâ€“Magnitude DLMS Adaptive Filters. Electronics (Switzerland), 2022, 11, 1007.	3.1	1
51	Enabling Fine Sample Rate Settings in DSOs with Time-Interleaved ADCs. Sensors, 2022, 22, 234.	3.8	1
52	A Binary Line Buffer Circuit Featuring Lossy Data Compression at Fixed Maximum Data Rate. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 121-134.	5.4	0