Ricardo FernÃ¡ndez-Pascual

List of Publications by Year
in descending order

21 papers	77 citations	1937685 4 h-index	1872680 6 g-index
21 all docs	21 docs citations	21 times ranked	53 citing authors

#	Article	IF	Citations
1	A Low Overhead Fault Tolerant Coherence Protocol for CMP Architectures. , 2007, , .		24
2	A fault-tolerant directory-based cache coherence protocol for CMP architectures. , 2008, , .		6
3	Managing resources dynamically in hybrid photonicâ€electronic networksâ€onâ€chip. Concurrency Computation Practice and Experience, 2014, 26, 2530-2550.	2.2	6
4	ICCI: In-Cache Coherence Information. IEEE Transactions on Computers, 2015, 64, 995-1014.	3.4	6
5	To be silent or not: on the impact of evictions of clean data in cache-coherent multicores. Journal of Supercomputing, 2017, 73, 4428-4443.	3.6	5
6	DAPSCO. Transactions on Architecture and Code Optimization, 2012, 8, 1-19.	2.0	4
7	Way-combining directory. , 2017, , .		4
8	Dealing with Transient Faults in the Interconnection Network of CMPs at the Cache Coherence Level. IEEE Transactions on Parallel and Distributed Systems, 2010, 21, 1117-1131.	5.6	3
9	Early Experiences with Separate Caches for Private and Shared Data. , 2015, , .		3
10	Are distributed sharing codes a solution to the scalability problem of coherence directories in manycores? An evaluation study. Journal of Supercomputing, 2016, 72, 612-638.	3.6	3
11	Extending Magny-Cours Cache Coherence. IEEE Transactions on Computers, 2012, 61, 593-606.	3.4	2
12	Way Combination for an Adaptive and Scalable Coherence Directory. IEEE Transactions on Parallel and Distributed Systems, 2019, 30, 2608-2623.	5.6	2
13	PfTouch: Concurrent page-fault handling for Intel restricted transactional memory. Journal of Parallel and Distributed Computing, 2020, 145, 111-123.	4.1	2
14	Concurrent Irrevocability in Best-Effort Hardware Transactional Memory. IEEE Transactions on Parallel and Distributed Systems, 2020, 31, 1301-1315.	5.6	2
15	Characterization of a List-Based Directory Cache Coherence Protocol for Manycore CMPs. Lecture Notes in Computer Science, 2014, , 254-265.	1.3	2
16	Extending the TokenCMP Cache Coherence Protocol for Low Overhead Fault Tolerance in CMP Architectures. IEEE Transactions on Parallel and Distributed Systems, 2008, 19, 1044-1056.	5.6	1
17	A dedicated privateâ€shared cache design for scalable multiprocessors. Concurrency Computation Practice and Experience, 2017, 29, e3871.	2.2	1
18	DeTraS: Delaying Stores for Friendly-Fire Mitigation in Hardware Transactional Memory. IEEE Transactions on Parallel and Distributed Systems, 2021, , 1-1.	5.6	1

#	Article	IF	Citations
19	Two proposals for the inclusion of directory information in the last-level private caches of glueless shared-memory multiprocessors. Journal of Parallel and Distributed Computing, 2008, 68, 1413-1424.	4.1	0
20	Analysing software prefetching opportunities in hardware transactional memory. Journal of Supercomputing, 0, , 1.	3.6	0
21	Analysis of the Interactions Between ILP and TLP With Hardware Transactional Memory. , 2022, , .		0