

Ashwin Ramachandran

List of Publications by Year in descending order

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#	ARTICLE	IF	CITATIONS
1	A PAM-8 Wireline Transceiver With Linearity Improvement Technique and a Time-Domain Receiver Side FFE in 65 nm CMOS. IEEE Journal of Solid-State Circuits, 2022, 57, 1527-1541.	5.4	8
2	Line Coding Techniques for Channel Equalization: Integrated Pulse-Width Modulation and Consecutive Digit Chopping. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 1192-1204.	5.4	6
3	A PAM-8 Wireline Transceiver with Receiver Side PWM (Time-Domain) Feed Forward Equalization Operating from 12-to-39.6Gb/s in 65nm CMOS. , 2019, , .		5
4	An iPWM Line-Coding-Based Wireline Transceiver With Clock -Domain Encoding for Compensating Up To 27-dB Loss While Operating at 0.5-to-0.9 V and 3-to-16 Gb/s in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2020, 55, 1946-1959.	5.4	2