

Gianluca Giustolisi

List of Publications by Year in descending order

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85
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86
docs citations

86
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686
citing authors

#	ARTICLE	IF	CITATIONS
1	A Biasing Approach to Design Ultra-Low-Power Standard-Cell-Based Analog Building Blocks for Nanometer SoCs. IEEE Access, 2022, 10, 25892-25900.	2.6	11
2	Design of CMOS three-stage amplifiers for near-to-minimum settling-time. Microelectronics Journal, 2021, 107, 104939.	1.1	8
3	Design of Three-Stage OTA Based on Settling-Time Requirements Including Large and Small Signal Behavior. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 998-1011.	3.5	13
4	Efficient Design Strategy for Optimizing the Settling Time in Three-Stage Amplifiers Including Small- and Large-Signal Behavior. Electronics (Switzerland), 2021, 10, 612.	1.8	4
5	A gm/ID-Based Design Strategy for IoT and Ultra-Low-Power OTAs with Fast-Settling and Large Capacitive Loads. Journal of Low Power Electronics and Applications, 2021, 11, 21.	1.3	7
6	Design of Three-Stage OTAs from Settling-Time and Slew-Rate Constraints. , 2021, , .		0
7	Behavioral Model of Silicon Photo-Multipliers Suitable for Transistor-Level Circuit Simulation. Electronics (Switzerland), 2021, 10, 1551.	1.8	0
8	Class-AB CMOS output stages suitable for low-voltage amplifiers in nanometer technologies. Microelectronics Journal, 2019, 92, 104597.	1.1	7
9	In-Depth Analysis of Pole-Zero Compensations in CMOS Operational Transconductance Amplifiers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4557-4570.	3.5	11
10	Optimized Charge Pump With Clock Booster for Reduced Rise Time or Silicon Area. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1977-1981.	2.2	30
11	Autonomous Energy-Efficient Wireless Sensor Network Platform for Home/Office Automation. IEEE Sensors Journal, 2019, 19, 3501-3512.	2.4	74
12	Bessel-like compensation of three-stage operational transconductance amplifiers. International Journal of Circuit Theory and Applications, 2018, 46, 729-747.	1.3	8
13	Settling-time oriented OTA design through the approximation of the ideal delay. , 2018, , .		1
14	Design of CMOS OTAs with Settling-Time Constraints. , 2018, , .		0
15	A Clock Boosted Charge Pump with Reduced Rise Time. , 2018, , .		2
16	Non-Inverting Class-AB CMOS Output Stage for Driving High-Capacitive Loads. , 2018, , .		1
17	High-dimensional dynamics in a single-transistor oscillator containing Feynman-Sierpiński resonators: Effect of fractal depth and irregularity. Chaos, 2018, 28, 093112.	1.0	8
18	Robust design of CMOS amplifiers oriented to settling-time specification. International Journal of Circuit Theory and Applications, 2017, 45, 1329-1348.	1.3	14

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19	Verilog-a modeling of Silicon Photo-Multipliers. , 2016, , .		2
20	Compensation strategy for high-speed three-stage switched-capacitor amplifiers. Electronics Letters, 2016, 52, 1202-1204.	0.5	11
21	Three-Stage Dynamic-Biased CMOS Amplifier With a Robust Optimization of the Settling Time. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2641-2651.	3.5	19
22	Integrated Quenching-and-Reset Circuit for Single-Photon Avalanche Diodes. IEEE Transactions on Instrumentation and Measurement, 2015, 64, 271-277.	2.4	24
23	Study of the role of particle-particle dipole interaction in dielectrophoretic devices for biomarkers identification. Lecture Notes in Electrical Engineering, 2015, , 9-12.	0.3	3
24	Theoretical and experimental study of the role of cell-cell dipole interaction in dielectrophoretic devices: application to polynomial electrodes. BioMedical Engineering OnLine, 2014, 13, 71.	1.3	18
25	Monolithic quenching-and-reset circuit for single-photon avalanche diodes. , 2014, , .		0
26	A simple extraction procedure for determining the electrical parameters in Silicon Photomultipliers. , 2013, , .		12
27	Logic gates dynamic modeling by means of an ultra-compact MOS model. , 2012, , .		0
28	An Accurate Ultra-Compact I^2V Model for Nanometer MOS Transistors With Applications on Digital Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 159-169.	3.5	28
29	Robust Miller Compensation With Current Amplifiers Applied to LDO Voltage Regulators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 1880-1893.	3.5	41
30	Behavioral modeling of statistical phenomena of single-photon avalanche diodes. International Journal of Circuit Theory and Applications, 2012, 40, 661-679.	1.3	38
31	Verilog-A modeling of SPAD statistical phenomena. , 2011, , .		11
32	A 50-mA 1-nF Low-Voltage Low-Dropout Voltage Regulator for SoC Applications. ETRI Journal, 2010, 32, 520-529.	1.2	12
33	Sample frequency effects on a new SC realization of fractional order integrator. , 2010, , .		3
34	On-chip low drop-out voltage regulator with NMOS power transistor and dynamic biasing technique. Analog Integrated Circuits and Signal Processing, 2009, 58, 81-90.	0.9	6
35	Dynamic-biased capacitor-free NMOS LDO voltage regulator. Electronics Letters, 2009, 45, 1140.	0.5	14
36	Design guidelines of CMOS class-AB output stages: a tutorial. Analog Integrated Circuits and Signal Processing, 2008, 56, 163-177.	0.9	6

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37	Low-voltage LDO Compensation Strategy based on Current Amplifiers. , 2008, , .		7
38	Modeling of EMI propagation in switched-capacitor ΣΔ A/D converter. , 2008, , .		0
39	High-Drive and Linear CMOS Class-AB Pseudo-Differential Amplifier. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 112-116.	2.3	12
40	Two-Stage OTA Design Based on Settling-Time Constraints. , 2007, , .		4
41	LDO compensation strategy based on current buffer/amplifiers. , 2007, , .		7
42	Resistance of Feedback Amplifiers: A Novel Representation. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 298-302.	2.3	5
43	Rosenstark-like Representation of Feedback Amplifier Resistance. , 2007, , .		0
44	NMOS Low Drop-Out Regulator with Dynamic Biasing. , 2006, , .		4
45	Techniques for evaluating harmonic distortion in class-AB output stages: A tutorial. Analog Integrated Circuits and Signal Processing, 2006, 47, 323-334.	0.9	2
46	Statistical modelling and design guidelines of CMOS current references. IET Circuits, Devices and Systems, 2006, 153, 559.	0.6	2
47	Comparison of methods for predicting distortion in class-AB stages. , 2005, , .		0
48	Design and comparison of very low-voltage CMOS output stages. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2005, 52, 1545-1556.	0.1	21
49	Analysis and optimization of a low-voltage class-AB output stage. , 2005, , .		0
50	Exploiting the high-frequency performance of low-voltage low-power SC filters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2004, 51, 77-84.	2.2	12
51	Analysis, modelling and optimization of a gain boosted telescopic amplifier. International Journal of Circuit Theory and Applications, 2003, 31, 513-528.	1.3	4
52	A low-voltage low-power voltage reference based on subthreshold MOSFETs. IEEE Journal of Solid-State Circuits, 2003, 38, 151-154.	3.5	239
53	A new method for harmonic distortion analysis in Class-AB stages. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2003, 50, 1559-1563.	0.1	8
54	A detailed analysis of power-supply noise attenuation in bandgap voltage references. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2003, 50, 185-197.	0.1	46

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55	An efficient fuzzy controller architecture in SC technique. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2002, 49, 208-218.	2.3	6
56	An approach to test the open-loop parameters of feedback amplifiers. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2002, 49, 70-75.	0.1	20
57	Resolution of a current-mode algorithmic analog-to-digital converter. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2002, 49, 1480-1486.	0.1	16
58	1.1-V CMOS output stage with excellent linearity. Electronics Letters, 2002, 38, 1299.	0.5	14
59	Current-mode A/D fuzzy converter. IEEE Transactions on Fuzzy Systems, 2002, 10, 533-540.	6.5	3
60	Analysis and optimization of a novel CMOS multiplier. International Journal of Circuit Theory and Applications, 2001, 29, 321-330.	1.3	1
61	Switched capacitor compatible minimum-maximum function. Electronics Letters, 2000, 36, 35.	0.5	2
62	Approach to the design of low-voltage SC filters. IET Circuits, Devices and Systems, 2000, 147, 196.	0.6	10
63	CMRR frequency response of CMOS operational transconductance amplifiers. IEEE Transactions on Instrumentation and Measurement, 2000, 49, 137-143.	2.4	19
64	A switched-capacitor compatible membership function block. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2000, 47, 1321-1325.	2.3	2
65	1.2-V CMOS op-amp with a dynamically biased output stage. IEEE Journal of Solid-State Circuits, 2000, 35, 632-636.	3.5	53
66	1.5 V power supply CMOS voltage squarer. Electronics Letters, 1997, 33, 1134.	0.5	10
67	Harmonic distortion in single-stage amplifiers. , 0, , .		8
68	A new method for evaluating harmonic distortion in push-pull output stages. , 0, , .		0
69	A novel 1.5-V CMOS mixer. , 0, , .		1
70	An approach to the design of low-voltage SC filters. , 0, , .		0
71	A novel method for determining open-loop parameters in feedback amplifiers. , 0, , .		0
72	A fuzzy membership function circuit in SC technique. , 0, , .		1

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73	VLSI implementation of a double-layer single cell RD-CNN for motion control. , 0, , .		3
74	A fuzzy controller for step-up DC/DC converters. , 0, , .		2
75	Detailed frequency analysis of power supply rejection in Brokaw bandgap. , 0, , .		10
76	Analysis of power supply noise attenuation in a PTAT current source. , 0, , .		1
77	Statistical analysis of the resolution in a current-mode ADC. , 0, , .		1
78	Analysis and optimization of gain-boosted telescopic amplifiers. , 0, , .		11
79	CMOS implementation of an extended CNN cell to deal with complex dynamics. , 0, , .		0
80	A novel 1-V class-AB transconductor for improving speed performance in SC applications. , 0, , .		14
81	Design of low-voltage low-power SC filters for high-frequency applications. , 0, , .		1
82	A 1-V CMOS output stage with high linearity. , 0, , .		1
83	Sigma-Delta A/D fuzzy converter. , 0, , .		0
84	Guidelines for designing class-AB output stages. , 0, , .		2
85	Statistical analysis of CMOS current reference. , 0, , .		0