Gianluca Giustolisi

List of Publications by Year
in descending order

85	1,032	566801 15	476904 29
papers	citations	h-index	g-index

86	86	86	686
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A low-voltage low-power voltage reference based on subthreshold MOSFETs. IEEE Journal of Solid-State Circuits, 2003, 38, 151-154.	3.5	239
2	Autonomous Energy-Efficient Wireless Sensor Network Platform for Home/Office Automation. IEEE Sensors Journal, 2019, 19, 3501-3512.	2.4	74
3	1.2-V CMOS op-amp with a dynamically biased output stage. IEEE Journal of Solid-State Circuits, 2000, 35, 632-636.	3.5	53
4	A detailed analysis of power-supply noise attenuation in bandgap voltage references. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2003, 50, 185-197.	0.1	46
5	Robust Miller Compensation With Current Amplifiers Applied to LDO Voltage Regulators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 1880-1893.	3.5	41
6	Behavioral modeling of statistical phenomena of singleâ€photon avalanche diodes. International Journal of Circuit Theory and Applications, 2012, 40, 661-679.	1.3	38
7	Optimized Charge Pump With Clock Booster for Reduced Rise Time or Silicon Area. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1977-1981.	2.2	30
8	An Accurate Ultra-Compact Iâ€“V Model for Nanometer MOS Transistors With Applications on Digital Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 159-169.	3.5	28
9	Integrated Quenching-and-Reset Circuit for Single-Photon Avalanche Diodes. IEEE Transactions on Instrumentation and Measurement, 2015, 64, 271-277.	2.4	24
10	Design and comparison of very low-voltage CMOS output stages. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2005, 52, 1545-1556.	0.1	21
11	An approach to test the open-loop parameters of feedback amplifiers. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2002, 49, 70-75.	0.1	20
12	CMRR frequency response of CMOS operational transconductance amplifiers. IEEE Transactions on Instrumentation and Measurement, 2000, 49, 137-143.	2.4	19
13	Three-Stage Dynamic-Biased CMOS Amplifier With a Robust Optimization of the Settling Time. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2641-2651.	3.5	19
14	Theoretical and experimental study of the role of cell-cell dipole interaction in dielectrophoretic devices: application to polynomial electrodes. BioMedical Engineering OnLine, 2014, 13, 71.	1.3	18
15	Resolution of a current-mode algorithmic analog-to-digital converter. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2002, 49, 1480-1486.	0.1	16
16	1â€…V CMOS output stage with excellent linearity. Electronics Letters, 2002, 38, 1299.	0.5	14
17	A novel 1-V class-AB transconductor for improving speed performance in SC applications. , 0, , .		14
18	Dynamic-biased capacitor-free NMOS LDO voltage regulator. Electronics Letters, 2009, 45, 1140.	0.5	14

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19	Robust design of CMOS amplifiers oriented to settlingâ€time specification. International Journal of Circuit Theory and Applications, 2017, 45, 1329-1348.	1.3	14
20	Design of Three-Stage OTA Based on Settling-Time Requirements Including Large and Small Signal Behavior. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 998-1011.	3.5	13
21	Exploiting the high-frequency performance of low-voltage low-power SC filters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2004, 51, 77-84.	2.2	12
22	High-Drive and Linear CMOS Class-AB Pseudo-Differential Amplifier. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 112-116.	2.3	12
23	A 50-mA 1-nF Low-Voltage Low-Dropout Voltage Regulator for SoC Applications. ETRI Journal, 2010, 32, 520-529.	1.2	12
24	A simple extraction procedure for determining the electrical parameters in Silicon Photomultipliers. , 2013, , .		12
25	Analysis and optimization of gain-boosted telescopic amplifiers. , 0, , .		11
26	Verilog-A modeling of SPAD statistical phenomena. , 2011, , .		11
27	Compensation strategy for highâ€speed threeâ€stage switchedâ€capacitor amplifiers. Electronics Letters, 2016, 52, 1202-1204.	0.5	11
28	In-Depth Analysis of Pole-Zero Compensations in CMOS Operational Transconductance Amplifiers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4557-4570.	3.5	11
29	A Biasing Approach to Design Ultra-Low-Power Standard-Cell-Based Analog Building Blocks for Nanometer SoCs. IEEE Access, 2022, 10, 25892-25900.	2.6	11
30	1.5 V power supply CMOS voltage squarer. Electronics Letters, 1997, 33, 1134.	0.5	10
31	Approach to the design of low-voltage SC filters. IET Circuits, Devices and Systems, 2000, 147, 196.	0.6	10
32	Detailed frequency analysis of power supply rejection in Brokaw bandgap. , 0, , .		10
33	Harmonic distortion in single-stage amplifiers. , 0, , .		8
34	A new method for harmonic distortion analysis in Class-AB stages. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2003, 50, 1559-1563.	0.1	8
35	Besselâ€like compensation of threeâ€stage operational transconductance amplifiers. International Journal of Circuit Theory and Applications, 2018, 46, 729-747.	1.3	8
36	High-dimensional dynamics in a single-transistor oscillator containing Feynman-SierpiÅ„ski resonators: Effect of fractal depth and irregularity. Chaos, 2018, 28, 093112.	1.0	8

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37	Design of CMOS three-stage amplifiers for near-to-minimum settling-time. Microelectronics Journal, 2021, 107, 104939.	1.1	8
38	LDO compensation strategy based on current buffer/amplifiers. , 2007, , .		7
39	Low-voltage LDO Compensation Strategy based on Current Amplifiers. , 2008, , .		7
40	Class-AB CMOS output stages suitable for low-voltage amplifiers in nanometer technologies. Microelectronics Journal, 2019, 92, 104597.	1.1	7
41	A gm/ID-Based Design Strategy for IoT and Ultra-Low-Power OTAs with Fast-Settling and Large Capacitive Loads. Journal of Low Power Electronics and Applications, 2021, 11, 21.	1.3	7
42	An efficient fuzzy controller architecture in SC technique. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2002, 49, 208-218.	2.3	6
43	Design guidelines of CMOS class-AB output stages: a tutorial. Analog Integrated Circuits and Signal Processing, 2008, 56, 163-177.	0.9	6
44	On-chip low drop-out voltage regulator with NMOS power transistor and dynamic biasing technique. Analog Integrated Circuits and Signal Processing, 2009, 58, 81-90.	0.9	6
45	Resistance of Feedback Amplifiers: A Novel Representation. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 298-302.	2.3	5
46	Analysis, modelling and optimization of a gain boosted telescopic amplifier. International Journal of Circuit Theory and Applications, 2003, 31, 513-528.	1.3	4
47	NMOS Low Drop-Out Regulator with Dynamic Biasing. , 2006, , .		4
48	Two-Stage OTA Design Based on Settling-Time Constraints. , 2007, , .		4
49	Efficient Design Strategy for Optimizing the Settling Time in Three-Stage Amplifiers Including Small- and Large-Signal Behavior. Electronics (Switzerland), 2021, 10, 612.	1.8	4
50	VLSI implementation of a double-layer single cell RD-CNN for motion control. , 0, , .		3
51	Current-mode A/D fuzzy converter. IEEE Transactions on Fuzzy Systems, 2002, 10, 533-540.	6.5	3
52	Sample frequency effects on a new SC realization of fractional order integrator. , 2010, , .		3
53	Study of the role of particle-particle dipole interaction in dielectrophoretic devices for biomarkers identification. Lecture Notes in Electrical Engineering, 2015, , 9-12.	0.3	3
54	Switched capacitor compatible minimum-maximum function. Electronics Letters, 2000, 36, 35.	0.5	2

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55	A switched-capacitor compatible membership function block. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2000, 47, 1321-1325.	2.3	2
56	A fuzzy controller for step-up DC/DC converters. , 0, , .		2
57	Guidelines for designing class-AB output stages. , 0, , .		2
58	Techniques for evaluating harmonic distortion in class-AB output stages: A tutorial. Analog Integrated Circuits and Signal Processing, 2006, 47, 323-334.	0.9	2
59	Statistical modelling and design guidelines of CMOS current references. IET Circuits, Devices and Systems, 2006, 153, 559.	0.6	2
60	Verilog-a modeling of Silicon Photo-Multipliers. , 2016, , .		2
61	A Clock Boosted Charge Pump with Reduced Rise Time. , 2018, , .		2
62	A novel 1.5-V CMOS mixer. , 0, , .		1
63	A fuzzy membership function circuit in SC technique. , 0, , .		1
64	Analysis and optimization of a novel CMOS multiplier. International Journal of Circuit Theory and Applications, 2001, 29, 321-330.	1.3	1
65	Analysis of power supply noise attenuation in a PTAT current source. , 0, , .		1
66	Statistical analysis of the resolution in a current-mode ADC. , 0, , .		1
67	Design of low-voltage low-power SC filters for high-frequency applications. , 0, , .		1
68	A 1-V CMOS output stage with high linearity. , 0, , .		1
69	Settling-time oriented OTA design through the approximation of the ideal delay. , 2018, , .		1
70	Non-Inverting Class-AB CMOS Output Stage for Driving High-Capacitive Loads. , 2018, , .		1
71	A new method for evaluating harmonic distortion in push-pull output stages. , 0, , .		0
72	An approach to the design of low-voltage SC filters. , 0, , .		0

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73	A novel method for determining open-loop parameters in feedback amplifiers. , 0, , .		0
74	CMOS implementation of an extended CNN cell to deal with complex dynamics. , 0, , .		0
75	Sigma-Delta A/D fuzzy converter. , 0, , .		0
76	Statistical analysis of CMOS current reference. , 0, , .		0
77	Comparison of methods for predicting distortion in class-AB stages. , 2005, , .		0
78	Analysis and optimization of a low-voltage class-AB output stage. , 2005, , .		0
79	Rosenstark-like Representation of Feedback Amplifier Resistance. , 2007, , .		0
80	Modeling of EMI propagation in switched-capacitor ΣΔ A/D converter. , 2008, , .		0
81	Logic gates dynamic modeling by means of an ultra-compact MOS model. , 2012, , .		0
82	Monolithic quenching-and-reset circuit for single-photon avalanche diodes. , 2014, , .		0
83	Design of CMOS OTAs with Settling-Time Constraints. , 2018, , .		0
84	Design of Three-Stage OTAs from Settling-Time and Slew-Rate Constraints. , 2021, , .		0
85	Behavioral Model of Silicon Photo-Multipliers Suitable for Transistor-Level Circuit Simulation. Electronics (Switzerland), 2021, 10, 1551.	1.8	0