

Pallab Dasgupta

List of Publications by Year in Descending Order

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.

70
papers

229
citations

7
h-index

10
g-index

92
ext. papers

315
ext. citations

1.9
avg, IF

3.22
L-index

#	Paper	IF	Citations
70	Safe and Stable RL (S2RL) Driving Policies Using Control Barrier and Control Lyapunov Functions. <i>IEEE Transactions on Intelligent Vehicles</i> , 2022 , 1-1	5	
69	(hf_0): A Hybrid Pitch Extraction Method for Multimodal Voice. <i>Circuits, Systems, and Signal Processing</i> , 2021 , 40, 262-275	2.2	
68	Usage-Driven Personalization of Power Management Logic. <i>IEEE Embedded Systems Letters</i> , 2021 , 13, 106-109	1	
67	SongF0: A Spectrum-Based Fundamental Frequency Estimation for Monophonic Songs. <i>Circuits, Systems, and Signal Processing</i> , 2021 , 40, 772-797	2.2	0
66	Performance-Driven Post-Processing of Control Loop Execution Schedules. <i>ACM Transactions on Design Automation of Electronic Systems</i> , 2021 , 26, 1-27	1.5	
65	SMT-Based Verification of Safety-Critical Embedded Control Software. <i>IEEE Embedded Systems Letters</i> , 2021 , 13, 138-141	1	0
64	Hierarchical Program-Triggered Reinforcement Learning Agents for Automated Driving. <i>IEEE Transactions on Intelligent Transportation Systems</i> , 2021 , 1-10	6.1	3
63	Migrating Assertions from Dense to Discrete Time. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2021 , 1-1	2.5	
62	A Methodology for Identification of Internal Nets for Improving Fault Coverage in Analog and Mixed Signal Circuits. <i>Journal of Electronic Testing: Theory and Applications (JETTA)</i> , 2020 , 36, 719-730	0.7	0
61	Assertions for Protecting Mixed-Signal Latency Contracts in Power Management. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2020 , 28, 1745-1756	2.6	1
60	Pattern Guided Integrated Scheduling and Routing in Multi-Hop Control Networks. <i>Transactions on Embedded Computing Systems</i> , 2020 , 19, 1-28	1.8	0
59	Recurrence in Dense-time AMS Assertions. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2020 , 1-1	2.5	1
58	An automated framework for exploitable fault identification in block ciphers. <i>Journal of Cryptographic Engineering</i> , 2019 , 9, 203-219	1.9	2
57	Synthesizing Performance-Aware (m, k)-Firm Control Execution Patterns Under Dropped Samples 2019 ,		1
56	ExpFault: An Automated Framework for Block Cipher Fault Analysis 2019 , 13-57		
55	Exploitable Fault Space Characterization: A Complementary Approach 2019 , 59-88		
54	Performance and energy aware robust specification of control execution patterns under dropped samples. <i>IET Computers and Digital Techniques</i> , 2019 , 13, 493-504	0.9	2

53	A Structured Approach for Rapid Identification of Fault-Sensitive Nets in Analog Circuits 2019 ,		1
52	Automatic Characterization of Exploitable Faults: A Machine Learning Approach. <i>IEEE Transactions on Information Forensics and Security</i> , 2019 , 14, 954-968	8	9
51	Interpreting Local Variables in AMS Assertions During Simulation. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2019 , 38, 980-984	2.5	3
50	Algorithmic approaches for optimizing electronic control unit time using multi-rate sampling. <i>Control Theory and Technology</i> , 2018 , 16, 173-190	1	2
49	Formal Feature Interpretation of Hybrid Systems. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2018 , 37, 2474-2484	2.5	3
48	Co-Synthesis of Loop Execution Patterns for Multihop Control Networks. <i>IEEE Embedded Systems Letters</i> , 2018 , 10, 111-114	1	2
47	Feature Based Coverage Analysis of AMS Circuits 2018 ,		2
46	Breaking Redundancy-Based Countermeasures with Random Faults and Power Side Channel 2018 ,		6
45	Solar Irradiance Prediction from Historical Trends Using Deep Neural Networks 2018 ,		2
44	Generating AMS Behavioral Models with Formal Guarantees on Feature Accuracy 2017 ,		1
43	ForFET: A Formal Feature Evaluation Tool for Hybrid Systems. <i>Lecture Notes in Computer Science</i> , 2017 , 437-445	0.9	1
42	Formal Methods for Validation and Test Point Prioritization in Railway Signaling Logic. <i>IEEE Transactions on Intelligent Transportation Systems</i> , 2017 , 18, 678-689	6.1	3
41	Route optimization for an electric vehicle with priority destinations 2017 ,		3
40	Feature Indented Assertions for Analog and Mixed-Signal Validation. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2016 , 35, 1928-1941	2.5	12
39	Formal Methods for Pattern Based Reliability Analysis in Embedded Systems 2015 ,		3
38	Monitoring AMS Simulation: From Assertions to Features 2015 ,		1
37	Adaptive sharing of sampling rates among software based controllers 2015 ,		1
36	Acceptance and random generation of event sequences under real time calculus constraints 2014 ,		1

35	Formal Hardware/Software Co-Verification of Embedded Power Controllers. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2014 , 33, 2025-2029	2.5	5
34	Synthesis of sampling modes for adaptive control 2014 ,		3
33	Formal Interpretation of Assertion-Based Features on AMS Designs. <i>IEEE Design and Test</i> , 2014 , 1-1	1.4	4
32	Formal Verification of Hardware / Software Power Management Strategies 2013 ,		7
31	Formal Methods for Early Analysis of Functional Reliability in Component-Based Embedded Applications. <i>IEEE Embedded Systems Letters</i> , 2013 , 5, 8-11	1	4
30	Reliability Guarantees in Automata-Based Scheduling for Embedded Control Software. <i>IEEE Embedded Systems Letters</i> , 2013 , 5, 17-20	1	0
29	POWER-TRUCTOR: An Integrated Tool Flow for Formal Verification and Coverage of Architectural Power Intent. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2013 , 32, 1801-1813	2.5	8
28	Counterexample Ranking Using Mined Invariants. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2013 , 32, 1978-1991	2.5	5
27	Early Analysis of Critical Faults: An Approach to Test Generation From Formal Specifications. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2012 , 31, 447-451	2.5	1
26	Cohesive Coverage Management: Simulation Meets Formal Methods. <i>Journal of Electronic Testing: Theory and Applications (JETTA)</i> , 2012 , 28, 449-468	0.7	1
25	A Generalized Theory for Formal Assertion Coverage 2012 ,		1
24	Assertion Aware Sampling Refinement: A Mixed-Signal Perspective. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2012 , 31, 1772-1776	2.5	4
23	Computing Minimal Debugging Windows in Failure Traces of AMS Assertions. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2012 , 31, 1776-1781	2.5	6
22	Synchronizing AMS Assertions with AMS Simulation. <i>ACM Transactions on Design Automation of Electronic Systems</i> , 2012 , 17, 1-25	1.5	7
21	Formal methods for ranking counterexamples through assumption mining 2012 ,		2
20	Auxiliary Specifications for Context-Sensitive Monitoring of AMS Assertions. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2011 , 30, 1446-1457	2.5	9
19	Auxiliary State Machines and Auxiliary Functions: Constructs for Extending AMS Assertions 2011 ,		2
18	Coverage Management with Inline Assertions and Formal Test Points 2010 ,		1

17	Leveraging UPF-extracted assertions for modeling and formal verification of architectural power intent 2010 ,		11
16	Policy Based Security Analysis in Enterprise Networks: A Formal Approach. <i>IEEE Transactions on Network and Service Management</i> , 2010 , 7, 231-243	4.8	20
15	Fault Analysis of Security Policy Implementations in Enterprise Networks 2009 ,		2
14	Instrumenting AMS assertion verification on commercial platforms. <i>ACM Transactions on Design Automation of Electronic Systems</i> , 2009 , 14, 1-47	1.5	19
13	An end to end correctness verification approach for application specific usage control 2009 ,		1
12	Inline Assertions - Embedding Formal Properties in a Test Bench 2009 ,		2
11	Incorporating local variables in mixed-signal assertions 2009 ,		5
10	A Verification framework for Analyzing Security Implementations in an Enterprise LAN 2009 ,		3
9	Accelerating Assertion Coverage With Adaptive Testbenches. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2008 , 27, 967-972	2.5	7
8	Satisfiability Models for Maximum Transition Power. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2008 , 16, 941-951	2.6	7
7	Cohesive Coverage Management for Simulation and Formal Property Verification 2008 ,		4
6	Bounded Delay Timing Analysis Using Boolean Satisfiability 2007 ,		3
5	The BUSpec platform for automated generation of verification aids for standard bus protocols 2004 ,		1
4	A Branching Time Temporal Framework for Quantitative Reasoning. <i>Journal of Automated Reasoning</i> , 2003 , 30, 205-232	1	1
3	Min-max event-triggered computation tree logic. <i>Sadhana - Academy Proceedings in Engineering Sciences</i> , 2002 , 27, 163-180	1	
2	Heuristic search strategies for multiobjective state space search. <i>Sadhana - Academy Proceedings in Engineering Sciences</i> , 1996 , 21, 263-290	1	
1	SAT based solutions for consistency problems in formal property specifications for open systems		2